



WHERE
INNOVATION
BEGINS

**DESIGN
AUTOMATION
CONFERENCE**

JULY 9-13, 2023

**MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA**

#60DAC



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DESIGN, AUTOMATION AND TEST IN EUROPE
THE EUROPEAN EVENT FOR ELECTRONIC SYSTEM DESIGN & TEST



25 – 27 MARCH 2024
VALENCIA, SPAIN

PALACIO DE CONGRESOS VALENCIA

DATE 2024 adopts the renewed format that was introduced in 2023. This means that DATE 2024 again uses an intensive three-day format, focussing on interaction as well as further strengthening the community. The vast majority of regular papers will be presented in technical sessions using short flash-presentations, where the emphasis is on poster-supported live interactions (in addition to the common full-length presentation videos available before, during and after the conference). By this, we make sure that the community can actually do what conferences are for: meeting, discussing and exchanging.

HIGHLIGHTS:

- › The 27th edition of the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the design, test and manufacturing of electronic circuits and systems hardware and software
- › Keynote speakers from academia and industry
- › Research paper presentations
- › Late Breaking Results paper presentations
- › Special days on emerging topics:
 - › Responsible and Robust AI
 - › Sustainable Computing
- › Special Initiative on Autonomous Systems Design
- › Focus Sessions on a broad range of hot academic and industrial topics
- › Unplugged Sessions
- › Embedded Tutorials
- › Half-day workshops on specialised and novel topics
- › Multi-Partner Project sessions
- › Young People Programme (PhD Forum, Careers Fair - Industry & Student Teams Fair & Design Contest, Careers Fair - Academia & Univeristy Fair)

WWW.DATE-CONFERENCE.COM

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IEEE Computer Society Test Technology Technical Community [TTTC]
IEEE Solid-State Circuits Society [SSCS]
IEEE Computer Society [IEEE CS]

DEAR COLLEAGUES AND FRIENDS,

Welcome to the 60th edition of DAC!

It was in May 1964 when the success story of this conference began, at that time called the SHARE design automation workshop with 17 presentations (on record) in two days.

Presentations like:

- “Verbal and graphical language for the AED system: A progress report” by Ross and Feldman,
- “A method for the best geometric placement of units on a plane” by M. Weindling,
- “AUTO CARD automated printed circuit board design” by F. B. Lavering,
- “Automatic test equipment production test in the design automation system” by C. M. Weems,

and others that defined what we understand today under the term Electronic Design Automation (EDA).

To put in perspective how visionary the founders and presenters of this first DAC edition were, we need to realize that the first commercially produced microprocessor would not be released until seven years after the first DAC. Even the first moon landing was still five years away.

There were several landmark inventions that had triggered the need for design automation:

- The first planar monolithic integrated circuit chip was demonstrated in 1960 and credited to Kilby and Noyce.
- The Quine–McCluskey algorithm for minimization of Boolean functions was developed from 1952-1956.
- In 1959 D. Engelbart studied the downscaling of integrated circuit size
- And in 1965, Gordon M. Moore presented his famous publication “Cramming more components onto integrated circuits”.

That was the ground on which DAC was built and the success story began. By the mid 1970s, the first place and route tools were developed and were published at DAC. In the late 1970s, the Mead–Conway VLSI chip design revolution began; the approach to specify a behaviour in a textual programming language and have the tools derive a specific physical design is still the basis of chip design today. Among the early landmark EDA tools was the ESPRESSO logic minimizer by Bob Brayton et al. in 1982. The success of this and other early academic EDA tools led to the first ever trade show for EDA – at DAC in 1982. Many inventions – EDA algorithms, methods and tools – have first been presented and published at DAC.

Now, with the 60th edition of the Design Automation Conference, DAC presents itself in the best shape ever: For the first time, the paper submissions have surpassed the 1,000 threshold – 1,156 to be precise.

In numerous international rankings, DAC is regarded the top conference in the EDA field. That is due to the true international character of DAC, with strong contributions from academic and industrial institutions alike, and with major contributions from the Americas, Asia and Europe.

Besides the technical program, DAC has a world-class trade show, and it has Engineering Tracks that bridge the academic world with the industrial world – the recipe for impactful, long-lasting success.

60 DAC has some novelties from which I want to introduce a few: The Most Influential Paper Award is presented for the first time this year. Given the impactful history of DAC, the award recognizes previously published DAC research papers that have shown long lasting impact in one or more of DAC’s core topics and that were published more than ten years ago. A novelty in the technical program are lightning talks that precede technical sessions and are given by recognized experts in the field; these serve as an introduction to the research area behind a technical session. On the exhibit floor, we’ll have over 130+ exhibitors showcasing their latest innovations and solutions. The RISC-V Zone will feature our community of designers, executives, researchers, and developers harnessing the power of the RISC-V open-source architecture for AIC- and FPGA-based designs. AI Hardware Alley will be a showcase of our exhibitors who are capitalizing on the growing artificial intelligence trends and the hardware that will accompany them.

WELCOME TO THE 60TH EDITION OF DAC!

Innovation at DAC is currently driven by machine learning and AI techniques that have opened new opportunities and that can provide significant improvements to EDA, as well as design tools and methods. Due to the success of machine learning and AI during the past five years at DAC, we now have a dedicated research tracks on AI/ML, which establishes DAC as a major conference for applied ML/AI.

We have four keynotes and four visionary talks as well as technical SKYTalk and TechTalk presentations. In total we have more than 100 sessions, including:

- 26 sessions on design (from heterogeneous SoCs, architectures, circuits, to emerging technologies)
- Sessions on AI/ML (software and system designs of neural network accelerators as well as the application of AI/machine learning techniques to advancing electronic design automation)
- More than 20 sessions on embedded software and systems (IoT, CPS, embedded memory, and edge computing)
- 12 sessions on cloud (design on cloud, ML, orchestration, and device life cycle management)

Please also visit the DAC Young Fellows Presentations, the DAC PhD Forum, plus the exciting educational sessions hosted at the DAC Pavilion that you can read more about in this program book.

DAC's unique exhibition will provide you the newest vendor developments in design and automation. With our twice-daily coffee breaks on the exhibition floor, you will be able to visit more than 120 exhibitors and the popular DAC Pavilion (Booth 2259) and Transformative Technologies Theater (Booth 1358). Please check out these other informative areas and activities:

- Design Infrastructure Alley
- RISC-V Zone
- Poster Gladiator Battles

Don't forget to download DAC's mobile app. It not only makes it easier for you to manage your schedule and activities at the show but also navigate the three floors of Moscone West.

Finally, I want to thank all who have helped to make 60 DAC possible: many thanks to my colleagues from the DAC EC, the TPC members of both the research and the Engineering Tracks, and all the volunteers and employees from the sponsor's societies/councils as well as the management companies.

I look forward to celebrating with you and meeting you in San Francisco in person!



JÖRG HENKEL

60 DAC General Chair

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CONFERENCE INFORMATION

Exhibit Hours

Exhibit Halls on Level 1 and Level 2

Monday

Exhibits Open: 10:00 am – 6:00 pm

Tuesday

Exhibits Open: 10:00 am – 6:00 pm

Wednesday

Exhibits Open: 10:00 am – 6:00 pm

Registration Hours

Location: Level 1 Lobby

Friday	1:00 pm – 4:00 pm
Saturday	12:00 pm – 5:00 pm
Sunday	7:00 am – 7:00 pm
Monday	7:00 am – 7:00 pm
Tuesday	8:00 am – 6:00 pm
Wednesday	8:00 am – 4:00 pm
Thursday	8:00 am – 11:00 am

Online Proceedings

To view the proceedings, please visit –
www.dac.com/proceedings60

Stay Connected

Enjoy complimentary WiFi at DAC:

Network Name: **DAC2023**

Password: **60DAC2023**

First Aid Room

Moscone West First Aid Office is located on the 1st Floor near the Howard Street entrance (behind registration).

Phone: 415.974.4159

REPORT ALL MEDICAL EMERGENCIES IMMEDIATELY

To report a medical emergency, call 511 on a white House Phone, or on a call phone dial 415.974.4021.

DAC Mobile App

You can download the 60th Design Automation Conference app in the following ways:

- Search your device's App Store for "DAC Conferences"
- Go to the following link: www.core-apps.com/dl/60dac

Once the DAC Conferences application has downloaded,

- Choose 60th Design Automation Conference.
- Select to download the event app.

Once you are in the app don't forget to set up your profile by going to the Publish My Profile icon. If you click the box to publish your profile your name (and picture if you upload one) will show in the Attendee icon. From there you can make "Friendships" with other attendees which will allow you to send messages, and set up private appointments.

For technical assistance please contact
support@core-apps.com

DAC DIRECTORY MAP: LEVEL 1



LEVEL 1 LOBBY

Registration

LEVEL 1 EXHIBIT HALL

Exhibits

Transformative Technology Theater (T-Cube)

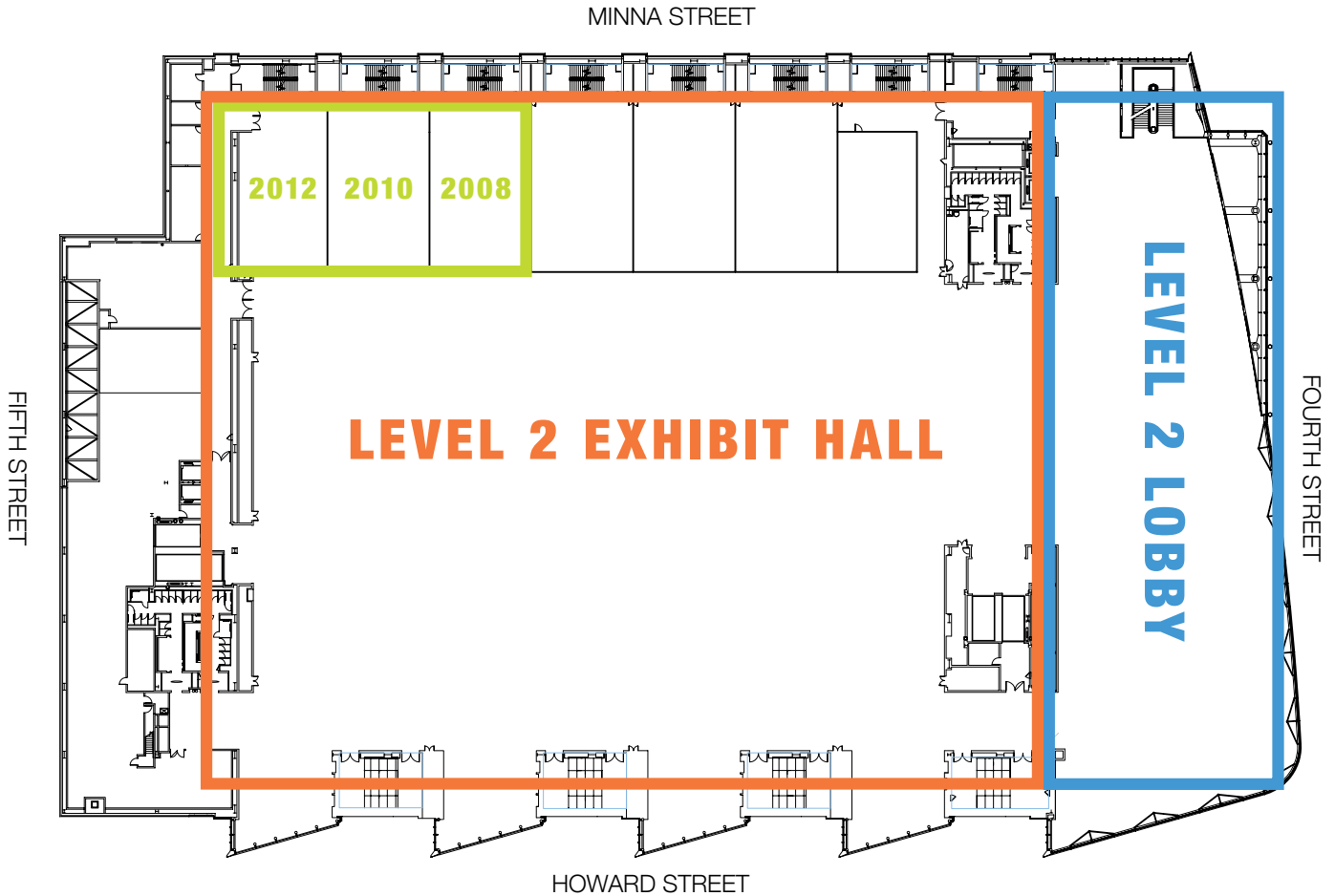
Design Infrastructure Alley

City Bytes & Beverages

Community Connection Zone

Conference Coffee Break

DAC DIRECTORY MAP: LEVEL 2



LEVEL 2 LOBBY

- Networking Receptions
- Work-in-Progress & Late Breaking Results Posters
- HACK at DAC
- Hands-on Training Sessions
- PhD Forum/University Demo

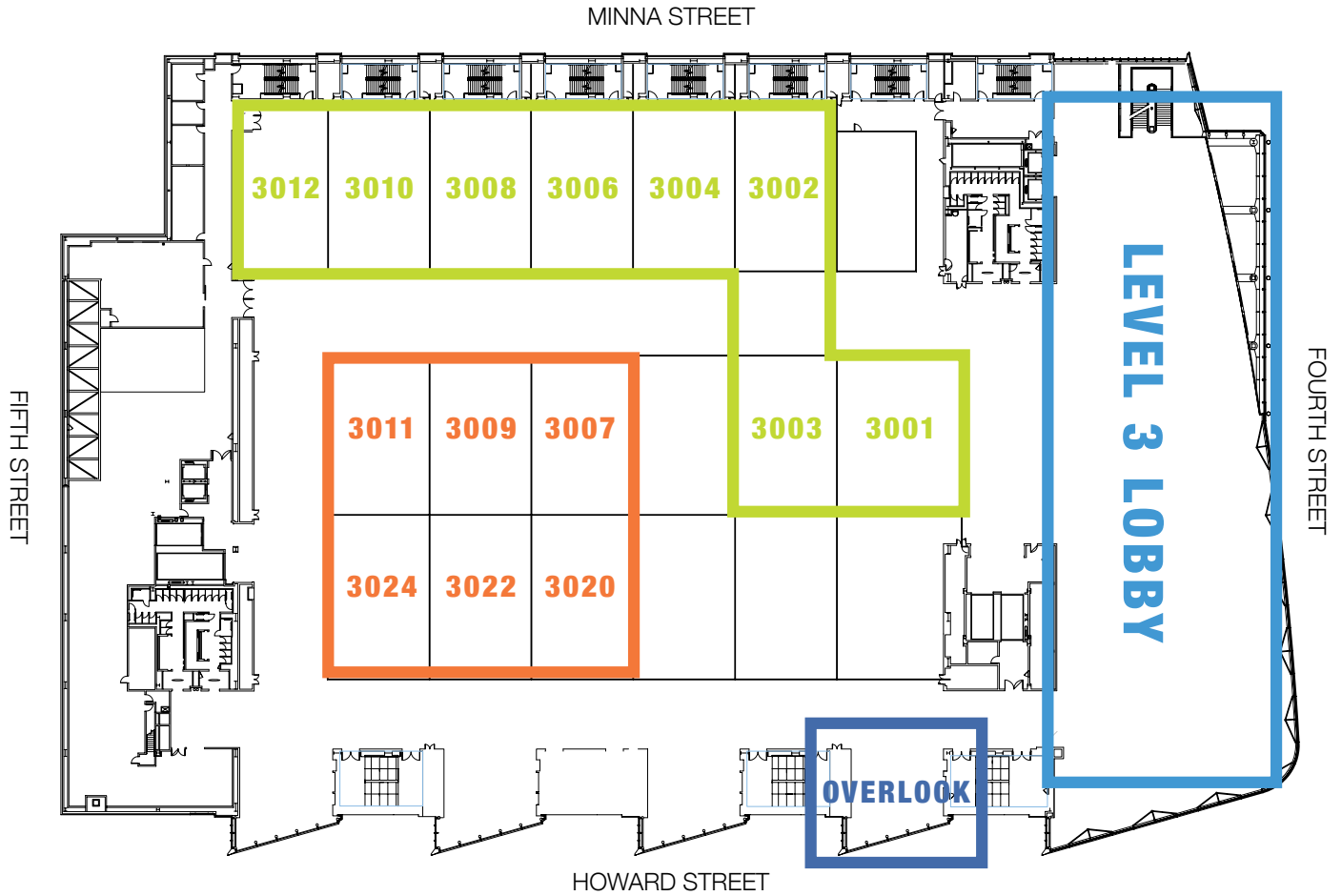
LEVEL 2 EXHIBIT HALL

- Exhibits
- DAC Pavilion
- Engineering Track Posters
- Press Room
- RISC-V Zone Theater

ROOMS 2008 – 2012

- Engineering Track Sessions

DAC DIRECTORY MAP: LEVEL 3



LEVEL 3 LOBBY

Welcome Reception

Speaker Breakfast

Career Development Day

ROOMS 3001 - 3012

Research Track Sessions

Birds of a Feather

ROOMS 3007, 3009, 3011

3020-3024

Keynote

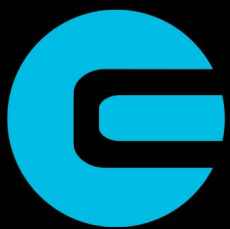
OVERLOOK

Speaker Ready Room

What will you Discover?



Circuit Cellar is the premier media resource for professional engineers, providing critical information on embedded and electronics technology.



circuit cellar

Inspiring the Evolution of Embedded Design

circuitcellar.com

DAC NETWORKING OPPORTUNITIES

Networking Receptions

Sunday, July 9th

Welcome Reception

6:00 pm – 7:00 pm | Level 3 Lobby

Monday, July 10th

Engineering Track Poster Session

5:00 pm – 6:00 pm | Exhibit Hall Level 2

Women in Tech Reception

6:00 pm – 7:30 pm | Level 2 Lobby

PhD Forum and University Demo

7:00 pm – 9:00 pm | Level 2 Lobby

Tuesday, July 11

Engineering Track Poster Session

5:00 pm – 6:00 pm | Exhibit Hall Level 2

Work-in-Progress Poster Session

6:00 pm – 7:00 pm | Level 2 Lobby

DAC 60 Celebration Party

6:00 pm – 9:00 pm | Level 2 Lobby

Wednesday, July 12

Engineering Track Poster Session and Networking Reception & Awards

5:00 pm – 6:00 pm | Exhibit Hall Level 2

Work-in-Progress/Late Breaking Results Poster Session

6:00 pm – 7:00 pm | Level 2 Lobby

60TH DAC Celebration

TUESDAY, JULY 11 • 6:00 PM – 9:00 PM • SECOND FLOOR LOBBY

FOOD, DRINKING, MUSIC, GAMES!

Connect with old friends and new as we celebrate 60 years of innovation at the biggest party DAC's ever thrown!

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KEYSIGHT

VISIONARY PRESENTATIONS



JOSEPH SAWICKI

EXECUTIVE VICE PRESIDENT, INTEGRATED CIRCUITS, ELECTRONIC DESIGN AUTOMATION, SIEMENS EDA

Systems 2030 – What's Needed to Succeed in the Next Decade of Design without Resorting to Human Cloning

Monday, July 10 | 9:00 am – 9:15 am

With the accelerating pace of semiconductor complexity, and the increasing software and semiconductor content in systems, traditional EDA levels of productivity increases are insufficient. As electronic systems expand to literally hold our lives in their virtual hands, good-enough no longer is. What is needed are solutions across the ecosystem that provide orders of magnitude improvements to productivity, allow new engineers to become experts in very short periods of time, facilitate cross domain collaboration and optimization, and minimize the design space that needs to be explored to ensure systems operate correctly.

In this talk we will explore the past, present and future of complex semiconductor systems design.

ABOUT: Joseph Sawicki is a leading expert in IC nanometer design and manufacturing challenges. Formerly responsible for Mentor's industry-leading design-to-silicon products, including the Calibre physical verification and DFM platform and Mentor's Tessent design-for-test product line, Sawicki now oversees all business units in the Siemens EDA IC segment. Sawicki joined Mentor Graphics in 1990 and has held previous positions in applications engineering, sales, marketing, and management. He holds a BSEE from the University of Rochester, an MBA from Northeastern University's High Technology Program, and has completed the Harvard Business School Advanced Management Program.



PRITH BANERJEE

CHIEF TECHNOLOGY OFFICER, ANSYS

Driving Engineering Simulation and Design with AI/ML

Tuesday, July 11 | 9:00 am – 9:15 am

Traditionally, engineered products were designed with mechanical and electrical CAD tools, simulated and validated for correctness with CAE tools, prototypes were fabricated and tested, and products were then manufactured at scale in factories. This process required long product cycles often spanning years to build a new product. Today, virtually unlimited computing and storage available from the cloud is available for generative design to explore 10,000 design choices in near real-time, verify these products accurately through simulation (eliminating the need to build physical prototypes) and manufacture the products using additive manufacturing and factory automation. In the past, simulation tools were used to model specific, solitary physics such as mechanical structures, fluid dynamics, or electromagnetic interactions by solving second order partial differential equations using numerical methods. Today, simulation tools solve multi-physics problems (fluid-structure-electromagnetics interactions) at scale using the most complex solvers. We will explore the use of AI, Machine Learning and Deep Learning to accelerate these engineering simulations. We have identified four broad use cases of AI/ML applied to simulation: (1) Automatic parameter selection of simulation solvers to improve workflows and designer productivity (2) Augmenting simulation with AI/ML to accelerate simulation by factors of 100X (3) The use of AI/ML based generative design techniques to explore 10,000 designs automatically (4) Business intelligence to help improve engineering workflows. My talk will address three broad categories of AI/ML applied to simulation. (1) Top-down methods where we apply an AI/ML framework to a black box solver to train the ML models to improve run time (2) Bottom-up methods where we deeply embed the AI/ML methods inside the physics of our solvers. (3) Reduced order models where the order of the solutions is reduced using AI/ML methods. We will illustrate each of these approaches on existing, commercial tools. As an example of a bottom-up approach, we will describe an ML-based Partial Differential Equation solver and apply it to accelerate Fluid Dynamics problems and will report our results on our Fluent CFD software. As an example of a top-down method, we will report on an ML framework to improve the productivity of any ML developer working in simulation. As an example of a reduced order model we will report on a hybrid digital twin tool called the Twin Builder. We will report on an end-to-end chip packaging solution using a combination of data-driven and physics-informed neural networks, as integrated within Ansys Redhawk/IcePak/Mechanical solutions for Conjugate Heat Transfer. We will describe approaches to support fast design exploration/optimization using ML frameworks. We will describe ML-enabled assistance in various steps of simulation workflows such as initial meshing, smart sub-modeling, user experience and automatic selection of parameters. We will report on automatically setting the best parameters in Fluent/Live AMG solver.

VISIONARY PRESENTATIONS *continued*

ABOUT: Prith Banerjee is the Chief Technology Officer of Ansys where he is responsible for leading the evolution of Ansys' Technology strategy and champion the company's next phase of innovation and growth. Formerly, he was Executive Vice President, Chief Technology Officer of Schneider Electric. Previously, Prith was Managing Director of Global Technology Research and Development at Accenture. Formerly, he was Chief Technology Officer and Executive Vice President of ABB. Earlier, he was Senior Vice President of Research at HP and Director of HP Labs. Formerly, Prith was Dean of the College of Engineering at the University of Illinois at Chicago. Formerly, he was the Walter P. Murphy Professor and Chairman of Electrical and Computer Engineering at Northwestern University. Prior to that, Prith was Professor of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. In 2000, he founded AccelChip, a developer of products for electronic design automation, which was acquired by Xilinx Inc. in 2006. During 2005-2011, he was Founder, Chairman and Chief Scientist of BINACHIP Inc., a developer of products in electronic design automation. FastCompany listed Prith in their 100 top business leaders in 2009. He is a Fellow of the AAAS, ACM and IEEE, and a recipient of the 1996 ASEE Terman Award, the 2001 Taylor Booth Award from IEEE, and the 1987 NSF Presidential Young Investigator Award. Prith earned a B.Tech. in electronics engineering from the Indian Institute of Technology,



LIP-BU TAN

CHAIRMAN OF WALDEN INTERNATIONAL AND FORMER CEO/EXECUTIVE CHAIRMAN OF CADENCE DESIGN SYSTEMS

Advancing Precision Medicine through Generative AI-driven Drug Development

Wednesday, July 12 | 9:00 am – 9:15 am

Traditionally, engineered products were designed with mechanical and electrical CAD tools, simulated and validated for correctness with CAE tools, prototypes were fabricated and tested, and products were then manufactured at scale in factories. This process required long product cycles often spanning years to build a new product. Today, virtually unlimited computing and storage available from the cloud is available for generative design to explore 10,000 design choices in near real-time, verify these products accurately through simulation (eliminating the need to build physical prototypes) and manufacture the products using additive manufacturing and factory automation. In the past, simulation tools were used to model specific, solitary physics such as mechanical structures, fluid dynamics, or electromagnetic interactions by solving second order partial differential equations using numerical methods. Today, simulation tools solve multi-physics problems (fluid-structure-electromagnetics interactions) at scale using the most complex solvers. We will explore the use of AI, Machine Learning and Deep Learning to accelerate these engineering simulations. We have identified four broad use cases of AI/ML applied to simulation: (1) Automatic parameter selection of simulation solvers to improve workflows and designer productivity (2) Augmenting simulation with AI/ML to accelerate simulation by factors of 100X (3) The use of AI/ML based generative design techniques to explore 10,000 designs automatically (4) Business intelligence to help improve engineering workflows. My talk will address three broad categories of AI/ML applied to simulation. (1) Top-down methods where we apply an AI/ML framework to a black box solver to train the ML models to improve run time (2) Bottom-up methods where we deeply embed the AI/ML methods inside the physics of our solvers. (3) Reduced order models where the order(?) of the solutions is reduced using AI/ML methods. We will illustrate each of these approaches on existing, commercial tools. As an example of a bottom-up approach, we will describe an ML-based Partial Differential Equation solver and apply it to accelerate Fluid Dynamics problems and will report our results on our Fluent CFD software. As an example of a top-down method, we will report on an ML framework to improve the productivity of any ML developer working in simulation. As an example of a reduced order model we will report on a hybrid digital twin tool called the Twin Builder. We will report on an end-to-end chip packaging solution using a combination of data-driven and physics-informed neural networks, as integrated within Ansys Redhawk/IcePak/Mechanical solutions for Conjugate Heat Transfer. We will describe approaches to support fast design exploration/optimization using ML frameworks. We will describe ML-enabled assistance in various steps of simulation workflows such as initial meshing, smart sub-modeling, user experience and automatic selection of parameters. We will report on automatically setting the best parameters in Fluent/Live AMG solver.

ABOUT: Lip-Bu Tan served as Executive Chair of the Board of Directors of Cadence since December 2021 and was a member of the Cadence Board of Directors since February 2004. He served as CEO of the company from 2009 to 2021 and as President from 2009 to 2017. He also serves as chairman of Walden International, the venture capital firm he founded in 1987, and is a founding managing partner of Walden Catalyst Ventures. Prior to joining Cadence, Mr. Tan was Vice President at Chappell & Co. and held management positions at EDS Nuclear and ECHO Energy. Mr. Tan is a member of The Business Council and serves on the boards of directors of Intel Corporation, Schneider Electric SE, Credo Technology Group Holding Ltd., and Green Hills Software. He also serves on the Board of Trustees and the School of Engineering Dean's Council at Carnegie Mellon University and on the University of California, Berkeley's Engineering Advisory Board. Mr. Tan received the Semiconductor Industry Association (SIA)'s 2022 Robert N. Noyce Award and the Global Semiconductor Alliance (GSA)'s 2016 Morris Chang Exemplary Leadership Award. Mr. Tan received a BS from Nanyang University in Singapore, an MS in nuclear engineering from the Massachusetts Institute of Technology, and an MBA from the University of San Francisco.

VISIONARY PRESENTATIONS *continued*



CECILIA METRA

PROFESSOR AND THE DEPUTY PRESIDENT OF THE SCHOOL OF ENGINEERING, UNIVERSITY OF BOLOGNA

AI Hardware Reliability and Safety Challenges to Enable the Future Metaverse

Thursday, July 13 | 9:00 am – 9:15 am

The Metaverse can be described as a new layer bridging the gap between the digital world and the real one. Today, we are assisting to the development of a significant variety of tools enabling a very accurate digital emulation of the real world (e.g., for product design), or an augmented reality experience (e.g., for education purposes), or the creation of a coupled digital-twin of a real entity (e.g., for product manufacturing and maintenance), etc. The Future Metaverse should include, interconnect and enhance all these already existing capabilities into a unified universe, consisting of interoperable digital and real worlds, with inclusive accessibility to all. Artificial Intelligence (AI) will play a fundamental role in enabling all of this, by providing human interaction with the metaverse (e.g., through speech and gesture recognition, object detection in images/videos, tactile sensing, etc.) and allowing a personalized experience in the metaverse (e.g., based on individual preferences, possible disabilities, etc.). Since AI will guide our integration in the future metaverse, reliability and safety of its implementing hardware with respect to faults and aging conditions possibly occurring during its operation in the field should be guaranteed. Safety and reliability challenges of the AI hardware to enable the future metaverse will be addressed.

ABOUT: Cecilia Metra is a Professor and the Deputy President of the School of Engineering at the University of Bologna, Italy, where she has worked since 1991, and from which she received the Laurea Degree in Electronic Engineering and the PhD in electronic engineering and computer science. In 2002, she was visiting faculty consultant for Intel Corporation. She is part of the Italian National Research Center on High Performance Computing, Big Data and Quantum Computing, and of the Italian Research Project on Security and Rights In the CyberSpace. She is 2022-2023 IEEE Director, Division V, and she was the 2019 President of the IEEE Computer Society. She is Co-Chair of the "IEEE Metaverse" Project of the IEEE Future Directions, and a member of several IEEE Committees, including the IEEE Conferences and the IEEE Award Committees. She was a member of the Board of Governors of the IEEE Computer Society and the IEEE CEDA. She was Editor-in-Chief of the IEEE Transactions on Emerging Topics in Computing, and Associate Editor-in-Chief of the IEEE Transactions on Computers. She contributed to numerous IEEE international conferences/symposia/workshops as General/Program Chair, Technical Program Committee member, and Keynote/Invited Speaker.

KEYNOTE PRESENTATIONS



ALBERTO L. SANGIOVANNI-VINCENTELLI

EDGAR L. AND HAROLD H. BUTTNER CHAIR OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCES AT THE UNIVERSITY OF CALIFORNIA AT BERKELEY

Corsi e Ricorsi: Here We Go Again

Monday, July 10 | 9:15 am – 10:00 am

In 2003, I argued that semiconductor and system design, and design automation, have evolved by way of a repeating pattern of intuitive approaches, great insights and rigorous, if conservative, methodologies that I called “Corsi e Ricorsi”, using the principles of Giambattista Vico, history philosopher of the XVI Century. Over the course of six decades, this phenomenon fueled an evolution in technologies and computational software that gradually freed silicon and system designers from the shackles of choice, empowering them to overcome 18 orders of magnitude of design complexity to date, never failing to bring the possibility horizon closer.

I will present the evolution of EDA as an effective and powerful early example of Artificial Intelligence, in its broadest sense as “the theory and development of computer systems able to perform tasks that normally require human intelligence”, separate the hype from reality, comment on the present frenzy around machine learning applied to EDA, and reassure our community that design automation engineering is, more than ever, one of the world’s most natural intelligence rich professions. Finally, I will discuss the challenges posed to EDA by the development of 3D integrated circuits and put them in the context of the evolution of packaging methods over the past 40 years.

ABOUT: Alberto Sangiovanni Vincentelli is the Edgar L. and Harold H. Buttner Chair of Electrical Engineering and Computer Sciences at the University of California at Berkeley. In 1980-1981, he was a Visiting Scientist at the Mathematical Sciences Department of the IBM T.J. Watson Research Center. In 1987, he was Visiting Professor at MIT. He is an author of over 800 papers, 17 books and 2 patents in the area of design tools and methodologies, large scale systems, embedded systems, hybrid systems and innovation. He was a co-founder of Cadence and Synopsys, the two leading companies in the area of Electronic Design Automation and the founder and Scientific Director of the PARADES Research Center in Rome.



HEIKE RIEL

IBM FELLOW, DEPARTMENT HEAD SCIENCE & TECHNOLOGY, IBM

Quantum Computing Roadmap

Tuesday, July 11 | 9:15 am – 10:00 am

Despite the continued advances of digital computing including accelerators for artificial intelligence, there are still many important and relevant mathematical problems that are intractable for classical computers. Quantum Computers are a radically different approach and open a new trajectory to evolve computation and enable solving difficult and complex problems. In the past years significant progress has been made toward understanding the scope of quantum computing, pushing its hardware and software technology, developing applications, and advancing error mitigation/correction protocols. An entire new computing system is built from the bottom up. Advancing the state-of-the-art as quickly as possible requires pursuing in parallel improvements in three key metrics – scale, quality, and speed of quantum systems, as well as simultaneously providing advanced capabilities to exploit the performance and make them easy to use. Integrating new technologies such as advanced packaging, high-density control signal delivery, developing advanced qubit control electronics have already enabled scaling of superconducting quantum processors to 433-qubits. Combined with increases in quality and speed this has driven significant improvements in the performance of quantum computers. Moreover, the computational capabilities of today’s quantum hardware can be extended by tight integration of quantum and classical resources using techniques like circuit knitting to accelerate the path towards quantum advantage. Developing approaches to connect individual quantum processors in various ways with classical as well as quantum communication links enables a modular approach to further scale quantum systems.

ABOUT: Heike Riel is IBM Fellow, Head of Science & Technology and Lead of IBM Research Quantum Europe at IBM Research. She is responsible for leading the research agenda of the Science & Technology department aiming to create scientific and technological breakthroughs in Quantum Computing, Physics of Artificial Intelligence, Nanoscience and Nanotechnology, Precision Diagnostics and Smart System Integration. She is a distinguished expert in nanotechnology and nanosciences and focuses her research on advancing the frontiers of information technology through the physical sciences. She contributed to advancements in the science and technology of nanoscale electronics, in particular the exploration and development of semiconducting nanowires and nanostructures for applications in future electronic and optoelectronic devices, in molecular electronics for future nanoscale switches and memory applications, and organic light-emitting diodes for display applications. Her current research interests include new materials and device concepts for future nanoelectronics for applications in quantum computing and neuromorphic computing. She also serves as the Deputy Director of the new Swiss National Competence Center for Research on Silicon Spin Qubits.

KEYNOTE PRESENTATIONS *continued*



WALDEN RHINES

PRESIDENT AND CEO, CORNAMI, INC.

Taking AI to the Next Level

Wednesday, July 12 | 9:15 am – 10:00 am

With forty years of involvement in product development of AI-related products, Dr. Rhines brings perspective to the emerging capabilities that will take AI to the next level of commercial reality. One of the most important enablers is the ability to protect data privacy and ownership while making the data available for intelligent queries. Rhines will address these and other issues that will drive the next wave in the AI revolution.

ABOUT: WALDEN C. (Wally) RHINES is President and CEO of Cornami, Inc., a fabless semiconductor and software company focused on fully homomorphic encryption. He was previously CEO of Mentor Graphics for 25 years and Chairman of the Board for 17 years. During his tenure at Mentor, revenue nearly quadrupled and market value of the company increased 10X. Prior to joining Mentor Graphics, Dr. Rhines was Executive Vice President, Semiconductor Group, responsible for TI's worldwide semiconductor business. Dr. Rhines has served on the boards of Cirrus Logic, QORVO, TriQuint Semiconductor, Global Logic, PTK Corp., Silvaco, Pallidus and as Chairman of the Electronic Design Automation Consortium (five two-year terms). He is a Lifetime Fellow of the IEEE. Dr. Rhines holds a Bachelor of Science degree in engineering from the University of Michigan, a Master of Science and PhD in materials science and engineering from Stanford University, an MBA from Southern Methodist University and Honorary Doctor of Technology degrees from the University of Florida and Nottingham Trent University. In 2021, the Global Semiconductor Alliance honored Dr. Rhines, with its prestigious Dr. Morris Chang Exemplary Leadership Award.



MARK HOROWITZ

YAHOO! FOUNDERS PROFESSOR, STANFORD UNIVERSITY

Life Post Moore's Law: The New CAD Frontier

Thursday, July 13 | 9:15 am – 10:00 am

For over 50 years, information technology has relied upon Moore's Law: providing, for the same cost, 2x the number of logic transistors that were possible a few years prior. For much of that time, the smaller devices also provided dramatic energy and performance improvement through Dennard Scaling, but that scaling ended over a decade ago. While technology scaling continues, per transistor cost is no longer scaling in the advanced nodes. In this post Moore's Law reality, further price/performance improvement follows only from improving the efficiency of applications using innovative hardware and software techniques. Unfortunately, this need for innovative system solutions runs smack into the enormous complexity of designing and debugging contemporary VLSI based hardware/software platforms; a task so large it has caused the industry to consolidate, moving it away from innovation. To overcome this challenge, we need to develop a new set of CAD tools to enable small groups of application experts to selectively extend the performance of those successful platforms. Like the ASIC revolution in the 1980s, the goal of these tools is to enable a new set of designers, then board level logic designers, now application experts, to leverage the power of customized silicon solutions. Like then, these tools won't initially be useful for current chip designers, but over time will underly all designs. In the 1980s to provide access to logic designers, the key technologies were logic synthesis, simulation, and placement/routing of their designs to gate arrays and std cells. Today, the key is to realize you are creating an "app" for an existing platform, and not creating the system solution from scratch (which is both too expensive and error prone), and to leverage the fact that modern "chips" are made of many chiplets. The new set of tools must provide a design window familiar to application developers, with similar descriptive, performance tuning, and debug capabilities. These new tools will be tied to highly capable platforms that are used as the foundation, like the appStore model for mobile phones. This talk will try to convince you this might be possible, and where innovative tools are needed.

ABOUT: Mark Horowitz is the Yahoo! Founders Professor at Stanford University and was chair of the Electrical Engineering Department from 2008 to 2012. He received his BS and MS in Electrical Engineering from MIT in 1978, and his PhD from Stanford in 1984. Dr. Horowitz has received many awards for his work and has broad research interests. He has worked on many processor designs, from early RISC chips and in 1990 he took leave from Stanford to help start Rambus Inc, a company designing high-bandwidth memory interface technology. His work at both Rambus and Stanford drove high-speed link designs for many decades. In the 2000s he started a collaboration with Marc Levoy in computational photography which led to light-field photography and microscopy. His current research includes updating both analog and digital design methods, agile hardware design, and applying engineering to biology. He remains interested in learning new things, and building interdisciplinary teams.



DR. DEV SHENOY

PRINCIPAL DIRECTOR FOR MICROELECTRONICS, DEPARTMENT OF DEFENSE

Microelectronics Security: A Growing National Imperative

Monday, July 10 | 1:00 pm – 1:45 pm | DAC Pavilion, Level 2 Exhibit Hall

The microelectronics industry continues to play a fundamental role in our nation's economic and national security, and technological standing. The recent CHIPS Act and ongoing Department of Defense initiatives such as the Rapid Assured Microelectronics Prototypes (RAMP) program, underscore the government's commitment to accelerating the nation's rapid pace of microelectronics innovation and enable U.S. development of the very best in circuit design, manufacturing, and packaging. But how are we ensuring security across the microelectronics supply chain?

Dr. Devanand Shenoy will provide insights into how a number of DoD and commercial initiatives and investments are strengthening our microelectronics security posture across the development and deployment of leading-edge microelectronics technologies. Learn more about how these programs present opportunities for the Design Automation Conference (DAC) community to participate in the strengthening of our microelectronics cybersecurity readiness.

ABOUT: Dr. Dev Shenoy joined the Office of the Under Secretary of Defense for Research and Engineering, OUSD(R&E), as the Principal Director for Microelectronics in July 2021. In this role, Dr. Shenoy is responsible for leading the Department of Defense's research and engineering efforts in Microelectronics. Prior to joining OUSD(R&E), Dr. Shenoy served as the Director of Microelectronics Innovation and as Director of Advanced Technologies at the University of Southern California's Information Sciences Institute. Prior to joining USC/ISI, Dr. Shenoy served as Chief Engineer in the Advanced Manufacturing Office at the Department of Energy (DOE) HQ. In that role, he co-authored DOE's 2015 QTR (Quadrennial Technology Review) that served as a blueprint for DOE's energy technology investments. Among other initiatives, Dr. Shenoy proposed and led a "Big Idea" for U.S. national security and economic competitiveness within the Office of EERE (Energy Efficiency and Renewable Energy) on "Beyond Moore Computing" with participation from eight DOE National Labs. Prior to joining DOE, Dr. Shenoy served as a Senior Advisor at the Manufacturing and Industrial Base Policy (MIBP) Office within the Office of the Secretary of Defense (OSD) as a detailee from the Army Night Vision and Sensors Directorate (NVESD) at Fort Belvoir. In that role, he co-led a Telecom initiative with the White House Office of Science and Technology Policy (OSTP) to explore U.S. opportunities in Optical networks.



DR. PAUL CUNNINGHAM

SENIOR VICE PRESIDENT AND GENERAL MANAGER, CADENCE DESIGN SYSTEMS

Entering a New Era with EDA 2.0 and AI-Driven Electronic System Design

Tuesday, July 11 | 1:00 pm – 1:45 pm | DAC Pavilion, Level 2 Exhibit Hall

At Cadence, we see a great opportunity for our industry to enter a new era of EDA 2.0, defined by AI-driven platforms that optimize horizontally across multiple runs of many tools throughout an entire system design program. Learn how EDA 2.0 is bringing all design and verification data together under a unified data platform—RTL, layouts, constraints, waveforms, coverage, reports, log files, state graphs, AI models, and metadata with our new Cadence Joint Enterprise Data and AI (JedAI) Platform.

ABOUT: Dr. Paul Cunningham has served as Senior Vice President and General Manager of the System Verification Group (SVG) since March 2021, running the division since 2018. His responsibilities include logic simulation, emulation, prototyping, formal verification, Verification IP, and functional debug. Prior to this role, Cunningham was responsible for Cadence's frontend digital design tools including logic synthesis and design-for-test. Dr. Cunningham joined Cadence in 2011 via the acquisition of Azuro, a startup developing concurrent physical optimization and useful skew clock tree synthesis technologies, where he was a co-founder and CEO. Dr. Cunningham holds a MS and a PhD in Computer Science from the University of Cambridge in the UK.

SKYTALK PRESENTATIONS *continued*



JEAN-PHILIPPE FRICKER

FOUNDER AND CHIEF SYSTEMS ARCHITECT, CEREBRAS SYSTEMS

The Cerebras CS-2: Designing an AI Accelerator Around the World's Largest 2.6 Trillion Transistor Chip

Wednesday, July 12 | 1:00 pm – 1:45 pm | DAC Pavilion, Level 2 Exhibit Hall

Today's exponential growth of neural networks is creating a demand for compute infrastructure that can't keep up with the traditional performance improvements gained through enhancements of semiconductors technology nodes. A co-designed approach is needed to keep up with the demand. We explore how increasing chip dimensions and resulting power and cooling densities are some of the enabling vectors of such co-design.

ABOUT: Jean-Philippe (J.P.) is Chief System Architect at Cerebras Systems. Before co-founding Cerebras, J.P. was Senior Hardware Architect at rack-scale flash array startup DSSD (acquired by EMC). Prior to DSSD, J.P. was Lead System Architect at SeaMicro where he designed three generations of fabric-based computer systems. Earlier in his career, J.P. was Director of Hardware Engineering at Alcatel-Lucent and Director of Hardware Engineering at Riverstone Networks. He holds an MS in Electrical Engineering from École Polytechnique Fédérale de Lausanne, Switzerland, and has authored 24 patents.



MOHAMED KASSEM

CTO AND CO-FOUNDER, EFABLESS.COM

Cloud But Not for Compute – A New Paradigm for Open IC Design

Monday, July 10 | 10:30 am – 11:15 am | Transformative Technology Theater, Level 1 Exhibit Hall

The advantages of cloud extend far beyond compute. Cloud enables secure collaboration at scale, and this is especially key for democratizing chip design. Cloud is the ideal platform for enabling open source reference designs in hardware, provide access to open-source/commercial tool suites, PDKs and everything else needed for end to end chip design. In this talk, you will hear about examples of entire communities leveraging an open platform for chip design, the rapidly evolving world of commercial chips based on open-source reference designs and inspirational success stories. The place where hardware and software developers, chip experts, students and researchers design, share, collaborate, fabricate and commercialize their own chips is here and NOW.

ABOUT: Mohamed Kassem is the CTO and Co-Founder of efabless.com, the first semiconductor company applying open community innovation to all aspects of product development. Prior to launching efabless in 2014, Mohamed held several technical and global leadership positions within Texas Instruments' Wireless Business Unit.

Mohamed joined TI in 2000 at the beginning of the digital telephony revolution fueled by the unprecedented integration of major phone functions on a single SoC. He led the first development of 45nm, 28nm analog & mixed-signal IP functions for wireless applications processors.

Mohamed holds a Masters degree in Electrical Engineering from the University of Waterloo, Ontario, Canada and A Bachelors degree in Communications & Electronics from Ain Shams University, Cairo, Egypt.



EDITH BEIGNÉ

RESEARCH DIRECTOR OF AR/VR SILICON, META REALITY LABS

Building the Metaverse: Augmented Reality Applications and Integrated Circuits Challenges

Monday, July 10 | 11:30 am – 12:30 pm | DAC Pavilion, Level 2 Exhibit Hall

Augmented reality is a set of technologies that will fundamentally change the way we interact with our environment. It represents a merging of the physical and the digital worlds into a rich, context aware and accessible user interface delivered through a socially acceptable form factor such as eyeglasses. One of the biggest challenges in realizing a comprehensive AR experience are the performance and form factor requiring new custom silicon. Innovations are mandatory to manage power consumption constraints and ensure both adequate battery life and a physically comfortable thermal envelope. This presentation reviews Augmented Reality and Virtual Reality applications and Silicon challenges.

ABOUT: Edith Beigné is the Research Director of AR/VR Silicon at Meta Reality Labs where she leads research projects driving the future of AR devices. Her main research interests are low power digital and mixed-signal circuits and design with emerging technologies. Over the past 20 years, she has been focusing her research on low power and adaptive circuit techniques, exploiting new design techniques and advanced technology nodes for different applications ranging from high performance multi-processors to ultra-low power SoC, and, more recently, AR/VR applications. She is the Executive vice chair of ISSCC 2024, was the technical chair of ISSCC 2022 and part of ISSCC TPC since 2014, part of VLSI symposium TPC between 2015 and 2020. Distinguished Lecturer for the SSCS in 2016/2017, Women-in-Circuits Committee chair and JSSC Associate Editor since 2018. She visited Stanford University in 2018 to research on emerging technologies and new architectures.

TECHTALK PRESENTATIONS *continued*



ROBERT WILLE

CHIEF SCIENTIFIC OFFICER, SOFTWARE COMPETENCE CENTER

Design Automation for Quantum Computing

Monday, July 10 | 3:00 pm – 3:45 pm | DAC Pavilion, Level 2 Exhibit Hall

Quantum computers have the potential to solve certain tasks that would take millennia to complete even with the fastest (conventional) supercomputer. Numerous quantum computing applications with a near-term perspective (e.g., for finance, chemistry, machine learning, optimization) and with a long-term perspective (i.e., cryptography, database search) are currently investigated.

The Design Automation Community needs to be ready for this! In fact, due to the radically different computational primitives, seemingly simple tasks in the design of corresponding computers and algorithms get substantially harder for quantum computing compared to conventional circuits and systems. This affects how we currently conduct design automation for quantum computing—or how we do not. In fact, established programming languages, synthesizers, design tools, test, or verification schemes do not work for quantum computers anymore. In many aspects, considering the design for quantum computers, we are back at square one. And this may lead to a situation where we may have quantum computers but no proper (automatic) methods that aid us in using their potential!

In this talk, we discuss how design automation can help and how we can get design automation experts excited for this emerging technology. To this end, we report from our long-standing expertise in this domain and our experiences on bridging the quantum computing and the EDA community. We illustrate that quantum computing is no "rocket science" and, using proper models and abstractions, design automation can make a huge difference. This is showcased by several methods and software tools which have been developed in the past years with design automation in mind. Finally, the integration of these methods, tools, and mindsets into entire ecosystems (covering the entire flow from applications to eventual realization) is presented.

ABOUT: Robert Wille is Full and Distinguished Professor at the Technical University of Munich, Germany, and Chief Scientific Officer at the Software Competence Center Hagenberg GmbH, Austria (a technology transfer company with more than 100 employees). For more than 15 years, he is working on topics in the domain of quantum computing and successfully established design automation concepts in this domain. The impact of his work is reflected by numerous awards such as Best Paper Awards, e.g., at TCAD and ICCAD, a DAC Under-40 Innovator Award, a Google Research Award, etc., collaborations with industrial partners in this domain, as well as his involvement in prestigious projects and initiatives, e.g., within the scheme of an ERC Consolidator Grant or the comprehensive quantum computing initiative of the Munich Quantum Valley.



MAJID AHADI DOLATSARA

SOFTWARE R&D ENGINEER, KEYSIGHT TECHNOLOGIES

Revolutionizing EDA: The Power of AI, ML, and NLP

Tuesday, July 11 | 10:30 am – 11:15 am | Transformative Technology Theater, Level 1 Exhibit Hall

The integration of AI, ML, and NLP techniques in EDA has the potential to significantly improve the efficiency, innovation, and quality of electronic systems. Customers in the semiconductor and EDA industries can benefit from reduced design time, increased reliability, and enhanced performance. This talk will draw upon use cases and research that have shown the integration of AI, ML, and NLP techniques in EDA has led to significant improvements in design accuracy. For example, ML algorithms have been used to optimize routing in complex circuits, while NLP techniques have been used to extract relevant design information from textual specifications. The talk will cover the use of unsupervised, supervised, and reinforcement learning techniques and NLP techniques in EDA tools and workflows.

ABOUT: Majid Ahadi Dolatsara received the B.Sc. degree in electrical engineering from K. N. Toosi University of Technology, Tehran, Iran, in 2013, the M.Sc. degree in electrical engineering from Colorado State University, Fort Collins, CO, USA, in 2016, and the Ph.D. degree in electrical and computer engineering from Georgia Institute of Technology, Atlanta, GA, USA, in 2021. He has won the Richard B. Schulz best paper award in transactions on electromagnetic compatibility in 2022.

He is currently employed by Keysight Technologies, Calabasas, CA, USA, as a research and development software engineer, working on electronic design automation software. His research interests include development of numerical and machine learning algorithms for high performance simulation in the area of signal and power integrity.

TECHTALK PRESENTATIONS *continued*



EZEKIEL 'ZEKE' WHEELER

YOUNG INNOVATOR, HAM RADIO OPERATOR (KJ7NLL)

DIY Orbital Tracking System for Space Communication: A Project to Contact the International Space Station

Tuesday, July 11 | 11:30 am – 12:30 pm | DAC Pavilion, Level 2 Exhibit Hall

Zeke Wheeler was 8 years-old when he asked his dad how he could call the astronauts on the International Space Station (ISS). This casual question resulted in a three-year epic STEM-learning adventure to contact the ISS, which included obtaining an FCC license to operate a radio, creating a satellite tracker using Legos, and researching, designing and building original circuit boards and antennas with his dad using Cadence Microwave Office. There have been trials as well as triumphs in this ongoing project of fortitude and resilience.

ABOUT: Zeke Wheeler is twelve years-old and demonstrated an early interest in engineering. In April he received the Best Presentation Award in the Multiphysics In-Design Analysis Track at CadenceLIVE 2023. Since 2020 he has been working to contact the International Space Station, using circuit boards and antennas designed in Microwave Office, and a satellite tracker made from Legos. He looks forward to sharing his project with the DAC community.



ERIK BERG

MICROSOFT

What ChatGPT and Generative AI means for Semiconductor Design and Development

Wednesday, July 12 | 11:30 am – 12:30 pm | DAC Pavilion, Level 2 Exhibit Hall

ChatGPT has generated a lot of excitement and speculation lately. People are asking how generative AI will affect us all. Questions around generative AI's potential and limitations are top of mind.

This talk will touch on how AI/ML is helping in the semiconductor industry, and what generative AI can do for the chip design process. How it is likely to affect how we build chips, and what it could mean for semiconductor productivity.

ABOUT: Erik Berg is a Principal Engineer at Microsoft and an innovative leader in the field of SoC verification.

With a career that has been guided by the ambition to maximize the impact of everyone on his team, Erik brings a unique perspective to his work. He is driven by the challenge of scaling verification teams and reducing risk through methodology, tooling, and automation initiatives. As part of Erik's passion for pushing the boundaries of hardware development, he leads Microsoft's Steering Group for the application of machine learning and artificial intelligence in this domain.

One of Erik's notable contributions to the field is the invention of the Debug Decision Tree (DDT) tool. Recognizing the critical importance of debug efficiency, he developed DDT to enhance debug knowledge sharing and automation and collaborated with Synopsys to launch DDT to the market in 2023.

Before joining Microsoft, Erik spent 19 years at Intel, holding verification roles covering IP, SOC, formal, power, and performance. His extensive experience across different domains has provided him with a comprehensive understanding of the complexities involved in creating cutting-edge hardware solutions.

Beyond his professional achievements, Erik holds a PhD from the University of Michigan, specializing in nanofabrication and single electron transistors. His academic background reflects his commitment to staying at the forefront of technological advancements.

IN MEMORIAM



Philip Raymond Moorby 1953 – 2022

Philip Raymond Moorby passed away on 15 September at the age of 69 in Rockport.

Phil was born in Birmingham UK on 25 April 1953, fourth child of Ken and Clarice Moorby. He received a degree in mathematics from the University of Southampton, UK followed by a master's degree in computer science in 1974 at Manchester University, UK.

In 1984 Phil joined a start-up in the US and moved to Massachusetts. Over the following years he developed and refined the Verilog simulator which became the gold standard for designing the transistor devices we use every day, and which pushed the limits of engineering, chemistry, and physics. Phil won many awards for his work. In 2016 he received a Fellow Award from the Computer History Museum joining Silicon Valley's most influential technologists.

Phil met his wife, Mary in 2013 and moved to Rockport to join her. He subsequently devoted his time to photography, woodworking, gardening and traveling worldwide with Mary.

Phil leaves behind his wife Mary, his daughter Jill, his stepchildren Brooke, Claire, and Brett whom he loved as his own, as well as his two sisters Jean and Kay, his brother Jack, and various grandchildren nieces and nephews.



Andres Takach 1964 – 2022

Andres was a research scientist at Mentor Graphics (now Siemens EDA) Catapult High-Level Synthesis group. He was also very active in the High-Level Synthesis community contributing in conferences, TPCs and reviewing papers. He was the chair of the OSCI standards committee for the SystemC Synthesizable Subset.



Richard Goering 1951 – 2023

Richard James Goering, was a technology journalist, who covered IC design and electronic design automation (EDA) starting in 1985. He wrote extensively about the EDA software technology that's essential for the design of all semiconductors and electronic systems today. In addition to in-depth stories about IC design technology, he wrote about business trends, legal issues, standards efforts, mergers and acquisitions, and the colorful people behind the design of electronic systems and ICs. Richard was best known for serving as EE Times' EDA editor for 17 years, where he wrote hundreds of articles for both the print and on-line editions of the electronics industry's premier weekly newspaper.

DAC AWARDS AND SCHOLARSHIPS

2023 DAC UNDER-40 INNOVATORS AWARD

Jianli Chen, Shanghai LEDA Technology Co., Ltd., Fudan University

Pierre-Emmanuel Gaillardon, University of Utah

Sriram Rajamanohar, Keysight

Yiyu Shi, University of Notre Dame

2023 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD

X. Sharon Hu, University of Notre Dame

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIP FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

Shane Williams, Princeton University

ACM/SIGDA

ACM FELLOWS

David Atienza, Swiss Federal Institute of Technology

Jörg Henkel, Karlsruhe Institute of Technology

Farinaz Koushanfar, UC San Diego

2023 ACM TODAES BEST PAPER AWARD

Atefeh Sohrabizadeh, **Cody (Hao) Yu**, **Min Gao**, **Jason Cong**, UCLA

ACM TODAES ROOKIE AUTHOR OF THE YEAR (RAY) AWARD

Yue Tang, University of Pittsburgh

BEST PAPER AWARD FOR ACM TRANSACTIONS ON RECONFIGURABLE TECHNOLOGY AND SYSTEMS (TRETS)

Niansong Zhang, **Xiang Chen**, **Nachiket Kapre**, University of Waterloo

ACM SIGDA DISTINGUISHED SERVICE AWARD

Tulika Mitra, National University of Singapore

Patrick Groeneveld, Cerebras Systems

ACM SIGDA OUTSTANDING NEW FACULTY AWARD

Tsung-Wei Huang, University of Utah

ACM SIGDA OUTSTANDING PH.D. DISSERTATION AWARD

Zhiyao Xie

Advisors: Yiran Chen and Hai Li, Duke University

SIGDA PIONEERING ACHIEVEMENT AWARD

Ron Rohrer, Southern Methodist University

SIGDA MERITORIOUS SERVICE AWARD

Robert Wille, Technical University of Munich

Lei Jiang, Indiana University Bloomington

Hui-Ru Jiang, National Taiwan University

Jeyavijayan (JV) Rajendran, Texas A&M University

IEEE/CEDA

2023 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO ELECTRONIC SYSTEMS DESIGN

For overall impact on Electronics industry through contributions to scan design for testability, related test automation.

Giovanni De Micheli, EPFL, Lausanne, Switzerland

IEEE CEDA OUTSTANDING SERVICE AWARD

For outstanding service to the EDA community as DAC General Chair in 2023.

Robert Oshana, NXP Semiconductors

IEEE FELLOWS

Sung Kyu Lim, Georgia Institute of Technology

Sherief Reda, Brown University

Zhiru Zhang, Cornell University

Norman Chang, ANSYS, Inc

Ryan Kastner, University of California-San Diego

IEEE/ACM A RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

Moshe Vardi, **Pierre Wolper**, Université de Liège

IEEE DONALD O. PEDERSON SOLID-STATE CIRCUITS AWARD

Ingrid Verbauwhede, KI Leuven

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS (TCAD) DONALD O. PEDERSON BEST PAPER AWARD

DNN+NeuroSim V2.0: An End-to-End Benchmarking Framework for Compute-in-Memory Accelerators for On-Chip Training

Xiaochen Peng, **Shanshi Huang**, **Hongwu Jiang**, **Anni Lu**, **Shimeng Yu**

IEEE ANDREW S. GROVE AWARD

H.-S. Philip Wong, Stanford University

DAC PAVILION SCHEDULE – BOOTH #2259

Monday, July 10

10:15 am – 11:15 am

PANEL: THE BEST OF BOTH WORLDS – BRIDGING THE GAP BETWEEN EDA, SYSTEM AND MANUFACTURING

Moderator: Jay Vleeschhouwer, Griffin Securities

Panelists: John Lee, Ansys; Tom Beckley, Cadence Design Systems; Brian Thompson, PTC; Tony Hemmelgarn, Siemens Digital Industries Software; Stephane Sireau, Dassault Systemes

11:30 am – 12:30 pm

TECHTALK: BUILDING THE METAVERSE: AUGMENTED REALITY APPLICATIONS AND INTEGRATED CIRCUITS CHALLENGES

Speaker: Edith Beigne, Meta

1:00 pm – 1:45 pm

SKYTALK: MICROELECTRONICS SECURITY: A GROWING NATIONAL IMPERATIVE

Speaker: Dr. Devanand Shenoy, U.S. Department of Defense

2:00 pm – 2:45 pm

PANEL: FAAS – HYPED UP NEW ACRONYM OR A WAY TO LEVEL THE SIMULATION PLAYING FIELD? THE OPPORTUNITIES AND CHALLENGES OF FAAS (FUNCTION AS A SERVICE) FOR ACCELERATING SIMULATION AND ANALYSIS.

Moderator: Ben Jordan, JordanDSP

Panelists: Rajath Narasimha, Keysight; Ryan Magruder, Rescale; Yi Cao, Meta Reality Labs; Kenneth Hill, Eviden

3:00 pm – 3:45 pm

TECHTALK: DESIGN AUTOMATION FOR QUANTUM COMPUTING

Speaker: Robert Wille, Software Competence Center

5:00 pm – 6:00 pm

GLADIATOR ARENA POSTER BATTLE

Tuesday, July 11

10:15 am – 11:15 am

ANALYST REVIEW: A VIEW FROM WALL STREET: THE STATE OF EDA

Speaker: Jay Vleeschhouwer, Griffin Securities

11:30 am – 12:30 pm

TECHTALK: DIY ORBITAL TRACKING SYSTEM FOR SPACE COMMUNICATION: A PROJECT TO CONTACT THE INTERNATIONAL SPACE STATION

Speaker: Zeke Wheeler, HAM Radio Operator (KJ7NLL)

1:00 pm – 1:45 pm

SKYTALK: ENTERING A NEW ERA WITH EDA 2.0 AND AI-DRIVEN ELECTRONIC SYSTEM DESIGN

Speaker: Paul Cunningham, System Verification Group

2:00 pm – 2:45 pm

PANEL: DESIGN CONSIDERATIONS AND TRADEOFFS FOR 2.5D CHIPLET SOLUTIONS

Moderator: Ed Sperling, Semiconductor Engineering

Panelists: Saif Alam, Movellus; Craig Bishop, Deca Technologies; Mark Kuemerle, Marvell; Tony Mastroianni, Siemens EDA

3:00 pm – 3:45 pm

PANEL: ASK ME ANYTHING WITH JOE COSTELLO AND WALLY RHINES

Moderator: Brian Fuller, Arm Ltd.

Panelists: Joe Costello, Metrics, Kwikbit, Arrikto, Acromove; Wally Rhines, Cornami, Inc.

5:00 pm – 6:00 pm

GLADIATOR ARENA POSTER BATTLE

Wednesday, July 12

10:15 am – 11:15 am

ANALYST REVIEW: THE AI HARDWARE SHOW LIVE: SILICON OR SURVIVAL

Speakers: Ian Cutress, More Than Moore; Sally Ward-Foxton, EE-Times

11:30 am – 12:30 pm

TECHTALK: WHAT CHATGPT AND GENERATIVE AI MEANS FOR SEMICONDUCTOR DESIGN AND DEVELOPMENT

Speaker: Erik Berg, Microsoft

1:00 pm – 1:45 pm

SKYTALK: THE CEREBRAS CS-2: DESIGNING AN AI ACCELERATOR AROUND THE WORLD'S LARGEST 2.6 TRILLION TRANSISTOR CHIP

Speaker: Jean-Philippe Fricker, Cerebras

2:00 pm – 2:45 pm

PANEL: IS SYSTEMS ENGINEERING THE SOLUTION TO THE LIMITS OF DENNARD SCALING AND MOORE'S LAW?

Moderator: Alix Paultre, Endeavor B2B

Panelists: Mark Malinoski, Siemens EDA; Larry Williams, Ansys; Brett Hillhouse, IBM; Pooria Yaghini, SpaceX

3:00 pm – 3:45 pm

PANEL: THE INDUSTRY 4.0 REVOLUTION OF SEMICONDUCTOR DESIGN

Moderator: Brian Bailey, Semiconductor Engineering

Panelists: Vijay Narayanan, proteanTecs; Mujtaba Hamid, Microsoft; KT Moore, Cadence Design Systems, Inc.; Mohit Gupta, Aphawave Semi

5:00 pm – 6:00 pm

GLADIATOR ARENA POSTER BATTLE AND ENGINEERING TRACK PRESENTATION AWARDS

2ND CAD FOR HARDWARE SECURITY WORKSHOP (CAD4SEC 2023)

Time: 8:00 AM – 5:00 PM

Event Type: Workshop

Topic Area(s): Security

Room: 3008, 3rd Floor

Organizer(s): Farimah Farahmandi, Mark Tehranipoor, University of Florida, Gainesville, FL

Security vulnerabilities in hardware designs may turn out to be catastrophic as it is almost impossible to patch them once the hardware design has been manufactured. The emerging and ever-increasing security vulnerabilities in modern/complex hardware designs have been studied in recent years, e.g., side-channel leakage, information leakage, access control violations, and malicious functionality. These attacks can virtually circumvent the security mechanisms built at pre-silicon and put the chips/systems at risk. Ensuring the security of hardware designs is challenging due to their huge complexity, aggressive time-to-markets, limited security-oriented knowledge of designers, high-recurring cost of maintaining large teams/devices, the difficulty of establishing security metrics, etc. In such a circumstance, it is difficult to manually analyze the design implementation in different levels of abstraction to identify potential vulnerabilities. Moreover, it is costly for a design house to keep many security experts. Therefore, the semiconductor industry and system integrators started to look for a set of metrics, reusable security solutions, and automatic computer-aided design (CAD) tools to aid analysis, identifying, root-causing, and mitigating SoC security problems.

The source of security vulnerabilities in hardware designs is manifold: (i) lack of in-depth security knowledge; (ii) design transformation (in IC supply chain or revisioning); (iii) Ever-increasing threat surfaces; (iv) unintentional aggressive optimization by CAD tools. In such circumstances, all hardware design teams must have automatic CAD solutions to be able to analyze the security of the hardware designs thoroughly, at all levels of abstraction, and against all existing threats (e.g., fault injection, side-channel, and hardware Trojan attacks). CAD tools must evaluate the security of the design in the pre-silicon stage and suggest possible countermeasures while it is possible to modify the design and address the potential vulnerabilities.

In consideration of the above challenges and possible solutions and continuation of the 1st (inauguration) CAD4Sec workshop successfully held last year at DAC'59 with more than 80 attendees, we sketch out the extension of this community-wide event by inviting the experts from the industry, academia, and government to expand the knowledge, to represent the need for, and to share the recent progress on the development of automatic security CAD solutions. Additionally, the 2nd CAD4Sec workshop will extend the size and the involvement of practical demonstrations on the recent CAD for security tools by both industries/academia. There will be a panel discussion consisting of experts in the field to talk about the roadmap for CAD for security development. In continuation to the 1st CAD4Sec workshop, the 2nd CAD4Sec workshop will contain several technical talks on the scope of metrics and CAD as the following:

- CAD for Power/Timing Side Channel Assessment
- CAD for Timing Side Channel Assessment
- CAD for Fault Injection Assessment

- CAD for Electromagnetic Radiation Assessment
- CAD for Security Property Generation
- CAD for Security-oriented Equivalency Checking
- CAD for Malicious Functionality
- CAD for Security Monitoring and Validation
- CAD for Security Verification of Advanced Packaging
- CAD for Secure Heterogeneous Integration Assessment
- CAD for Physical Probing Assessment
- CAD for (Anti-)Reverse Engineering Assessment

4TH ROAD4NN WORKSHOP: RESEARCH OPEN AUTOMATIC DESIGN FOR NEURAL NETWORKS

Time: 8:00 AM – 5:00 PM

Event Type: Workshop

Topic Area(s): AI

Room: 3003, 3rd Floor

Organizer(s): Zhenman Fang, Simon Fraser University, Vancouver, Canada; Yanzhi Wang, Northeastern University, Boston, MA; Linghao Song, University of California, Los Angeles, CA

In the past decade, machine learning, especially neural network based deep learning, has achieved an amazing success. Various neural networks, such as CNNs, RNNs, LSTMs, Transformers, Vision Transformers, GNNs, and SNNs, have been deployed for various industrial applications like image classification, speech recognition, and automated control. On one hand, there is a very fast algorithm evolution of neural network models, and almost every week there is a new model from a major academic and/or industry institute. On the other hand, all major industry giants have been developing and/or deploying specialized hardware platforms to accelerate the performance and energy-efficiency of neural networks across the cloud and edge devices. This includes Nvidia GPU, Intel Nervana/Habana/Loihi ASICs, Xilinx FPGAs, Google TPUs, Microsoft Brainwave, Amazon Inferentia, to name just a few. However, there is a significant gap between the fast algorithm evolution and staggering hardware development, hence calling for broader participation in software-hardware co-design from both academia and industry.

In this workshop, we focus on the research open automatic design for neural networks, a holistic open source approach to general-purpose computer systems broadly inspired by neural networks. More specifically, we discuss full stack open source infrastructure support to develop and deploy novel neural networks, including novel algorithms and applications, hardware architectures and emerging devices, as well as programming, system, and tool support. We plan to bring together academic and industry experts to share their experience, discuss challenges they face as well as potential focus areas for the community. Below is the planned workshop content.

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

IN-MEMORY ARCHITECTURES AND COMPUTING APPLICATIONS WORKSHOP (IMACAW) – 2ND EDITION

Time: 8:00 AM – 5:00 PM

Event Type: Workshop

Topic Area(s): Design

Room: 3004, 3rd Floor

Organizer(s): Nima TaheriNejad, Heidelberg University, Heidelberg, Germany; Alberto Bosio, Lyon Institute of Nanotechnology, Lyon, France; Deliang Fan, Arizona State University, Tempe, AZ

Today's computer architectures and device technologies used to manufacture them are facing major challenges, rendering them incapable of delivering the performances required by complex applications such as Big-Data processing and Artificial Intelligence (AI). The iMACAW workshop aims at providing a forum to discuss In-Memory-Computing (as an alternative architecture) and its potential applications. To this end, we take a cross-layer and cross-technology approach covering State-of-the-Art (SoA) works that use SRAM, DRAM, FLASH, RRAM, PCM, MRAM, or FeFET as their memory technology. The workshop also aims at reinforcing the In-Memory-Computing (IMC) community and at offering a holistic vision of this emerging computing paradigm to the design automation communities.

This workshop will provide an opportunity for the audience to listen to invited speakers who are pioneers of the field, learn from them, ask questions, and interact with them. Open submission contributors also get the opportunity to share their knowledge, present their most-recent work, and their work in progress with the community, interact with other experts in the field, and receive feedback.

SSH-SOC: SECURITY AND SAFETY IN HETEROGENEOUS OPEN SYSTEM-ON-CHIP PLATFORMS

Time: 8:00 AM – 5:00 PM

Event Type: Workshop

Topic Area(s): Security

Room: 3010, 3rd Floor

Organizer(s): Francesco Restuccia, University of California, San Diego, San Diego, CA; Biruk Seyoum, Columbia University, New York, NY; Davide Rossi, University of Bologna, Bologna, Italy; Luca Benini, ETH Zürich, Switzerland

The diminishing returns of technology scaling on performance have paved the way for innovation in computer architecture towards heterogeneous, domain-specific architectures.

Modern systems increasingly comprise domain-specific accelerators as well as specialized system components (buses, network-on-chip, peripherals, sensors, etc..) to efficiently handle the complex and computationally demanding workloads.

A popular approach to reduce the SoC design complexity involves a hierarchical strategy of differentiating the system design effort for the components of the heterogeneous architecture. This includes: (i) expensive in-house RTL development for the most critical modules, (ii) leveraging the most recent high-level synthesis (HLS) tools, and/or (iii) outsourcing highly-specialized third-party intellectual property (IP) modules to reduce cost and development time.

Despite its benefits, a diversified design methodology exacerbates the system integration challenge. Furthermore, several recent works have demonstrated how non-careful system integration can lead to dangerous conditions capable of affecting the security, safety, and performance of the system. This can derive from the combination of multiple aspects involving development bugs, lack of specifications, superficial verifications of the behavior of the IP components at the system level, and scarcity of mechanisms supporting the safe and secure system execution.

Such challenges require novel approaches in the design and verification process, in particular when dealing with the strict safety and security requirements of mission-critical systems. The research community can have a disruptive role in facing these challenges – the availability of the full codebase of multiple mature open hardware architectures and reconfigurable platforms represents an unprecedented opportunity for the development, testing, and native integration of novel mechanisms, tools, and analysis supporting security, safety, and performance efficiency for the development of the next-generation of systems.

This workshop welcomes work-in-progress contributions and novel directions to tackle the challenges and profit from the opportunities provided by open hardware designs and architectures for the development of next-generation heterogeneous SoCs. The topics for the workshop include, but are not limited to:

- Security verification for hardware designs and system architectures
- Architectural aspects of secure system integration
- Secure system integration of third-party hardware components
- Automated firmware generation supporting secure system execution
- Security aspects of reconfigurable designs
- Time-predictable system execution in open-hardware designs
- Performance analysis, timing analysis, and worst-case analysis supporting time-predictable system execution and/or communications in open-hardware designs
- Automated firmware generation supporting time-predictable execution
- Fault tolerance and execution in harsh conditions leveraging open-hardware designs
- System architectures and methodologies supporting energy efficient/performant system execution in open-hardware designs
- Hardware/software co-design, co-integration and co-verification of open-source processors, accelerators, and components
- Open architectures for reconfigurable platforms and open CAD tools
- Tools and analysis for open FPGAs and reconfigurable platforms

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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THE SIXTH INTERNATIONAL WORKSHOP ON DESIGN AUTOMATION FOR CYBER-PHYSICAL SYSTEMS (DACPS)

Time: 8:00 AM – 5:00 PM

Event Type: Workshop

Topic Area(s): Embedded Systems and Software

Room: 3002, 3rd Floor

Organizer(s): Xun Jiao, Villanova University, Villanova, PA; Chao Huang, University of Liverpool, United Kingdom

Cyber-Physical Systems (CPS) are characterized by the strong interactions between cyber and physical components. CPS system examples include automotive and transportation systems, avionics systems, smart home, building and community, smart battery and energy systems, robotic systems, cyber-physical biochip, wearable devices, and so on. Due to the deeply complex intertwining among different components, CPS designs pose fundamental challenges in multiple aspects such as safety, performance, security, reliability, fault tolerance, extensibility, and energy consumption. Developing innovative design automation techniques, algorithms and tools is imperative to address the unique challenges in CPS design and operation, such as the fast increase of system scale and complexity, the close interactions with dynamic physical environment and human activities, the significant uncertainties in sensor readings, the employment of distributed architectural platforms, and the tight resource and timing constraints. This workshop will present the state-of-the-art research results on the topic of design automation for CPS/IoT systems, introduce practical challenges and promising solutions in various industry sectors, and stimulate CAD researchers to participate in the interdisciplinary CPS/IoT research.

WORKSHOP ON CHIPLET-BASED HETEROGENEOUS INTEGRATION AND CO-DESIGN (CHICO)

Time: 8:00 AM – 5:00 PM

Event Type: Workshop

Topic Area(s): EDA

Room: 3006, 3rd Floor

Organizer(s): Yu Cao, Arizona State University, Tempe, AZ; Puneet Gupta, University of California, Los Angeles, CA

Contemporary microelectronic design is facing tremendous challenges in memory bandwidth, processing speed and power consumption. Although recent advances in monolithic design (e.g., near-memory and in-memory computing) help relieve some issues, the scaling trend is still lagging behind the ever-increasing demand of AI, HPC and other applications. In this context, technological innovations beyond a monolithic chip, such as 2.5D and 3D packaging at the macro and micro levels, are critical to enabling heterogeneous integration with various types of chiplets, and bringing significant performance and cost benefits for future systems. Such a paradigm shift further drives new innovations on chiplet IPs, heterogeneous architectures and system mapping.

This workshop is designed to be a forum that is highly interactive, timely and informative, on the related topics:

1. Roadmap and technology perspectives of heterogeneous integration
2. IP definition for chiplets
3. Signaling interface cross chiplets
4. Network topology for data movement
5. Design solutions for power delivery
6. Thermal management
7. Testing in a heterogeneous system
8. High-level synthesis for the chiplet system
9. Architectural innovations
10. Ecosystems of IPs and EDA tools

Learn more at <http://nimo.asu.edu/chico>

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PROGRAM

Monday, July 10, 2023

WHAT THE NEXT SEMICONDUCTOR UPCYCLE WILL LOOK LIKE FOR EDA

Time: 5:00 PM – 6:00 PM
Event Type: Special Session
Topic Area: EDA
Room: 3002, 3rd Floor

Organizer: Charles Shi, PhD, Needham & Company LLC

Over the past year, EDA proved to be the only semiconductor segment that escaped the industry downturn. As we look forward to the next semiconductor upcycle, we believe EDA's outperformance will continue, as the fundamental forces that shape the industry, e.g., the slowdown of Moore's Law, the rise of domain-specific computing, and the democratization of chip design across the technology ecosystem, will maintain and potentially further accelerate EDA's strong growth over at least the next 3-4 years.

MONDAY KEYNOTE: ALBERTO L. SANGIOVANNI-VINCENTELLI AND VISIONARY TALK: JOSEPH SAWICKI

Time: 8:40 AM – 10:00 AM
Event Type: Keynote, Visionary Talk
Topic Area(s):
Room: 3020, 3rd Floor

INTRODUCTION AND AWARDS

VISIONARY TALK: SYSTEMS 2030 – WHAT'S NEEDED TO SUCCEED IN THE NEXT DECADE OF DESIGN WITHOUT RESORTING TO HUMAN CLONING

Joseph Sawicki, Siemens EDA, Portland, OR

KEYNOTE: CORSI E RICORSI: HERE WE GO AGAIN

Alberto Sangiovanni-Vincentelli, University of California, Berkeley, CA

BEST OF BOTH WORLDS – BRIDGING THE GAP BETWEEN EDA, SYSTEM AND MANUFACTURING

Time: 10:15 AM – 11:15 AM
Event Type: DAC Pavilion Panel
Topic Area(s): Back-End Design
Room: DAC Pavilion, Level 2 Exhibit Hall

Panelists: Jay Vleeschhouwer, Griffin Securities, New York, NY; John Lee, Ansys, San Jose, CA; Tom Beckley, Cadence Design Systems, Inc., Pittsburgh, PA; Brian Thompson, PTC, Boston, MA; Tony Hemmelgarn, Siemens EDA, Livonia, MI; Stephane Sireau, Dassault Systemes

CLOUD BUT NOT FOR COMPUTE – A NEW PARADIGM FOR OPEN IC DESIGN

Time: 10:30 AM – 11:15 AM
Event Type: Transformative Technologies Theater
Topic Area(s): Cloud
Room: Transformative Technologies Theater, Level 1 Exhibit Hall

The advantages of cloud extend far beyond compute. Cloud enables secure collaboration at scale, and this is especially key for democratizing chip design. Cloud is the ideal platform for enabling open source reference designs in hardware, provide access to open-source/commercial tool suites, PDKs and everything else needed for end to end chip design. In this talk, you will hear about examples of entire communities leveraging an open platform for chip design, the rapidly evolving world of commercial chips based on open-source reference designs and inspirational success stories. The place where hardware and software developers, chip experts, students and researchers design, share, collaborate, fabricate and commercialize their own chips is here and NOW.

Presenter: Mohamed Kassem, eFabless

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Engineering Track

HOT HOT CHIPS: ENSURING STABLE POWER DELIVERY OF AN SOC SYSTEM

Time: 10:30 AM – 12:00 PM

Event Type: Engineering Tracks

Topic Area(s): Back-End Design

Room: 2008, Level 2

Session Chair(s): Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., IEEE

Power Delivery and Thermal Management are now foundations to make a Hot Chip look cool in its working. Gather around the fire to learn stories from the adventures of fellow travelers.

IR-DROP AWARE POWER LAYOUT OPTIMIZATION METHODOLOGY FOR FULL-CUSTOM DESIGN

Seonghyeon Park, Samsung Electronics, Hwaseong, South Korea

AUTOMATED MIMCAP INSERTION SOLUTION FOR TURN-AROUND-TIME REDUCTION

Ingeol Lee, Kiwon Yoon, Jongho Kim, Jun Seomun, **Sangyun Kim**, Samsung Electronics, Hwaseong, South Korea

THERMAL AWARE ON-DIE ELECTRICAL ANALYSIS

Anubhav Johri, Analog Devices, Uttar Pradesh, India

HIGH BANDWIDTH MEMORY (HBM3-7.2GBPS) 2.5D-IC INTEGRATION WITH SIGNAL INTERCONNECTS AND POWER DISTRIBUTED NETWORKS DESIGN-OPTIMIZATION

Sam Yang, **Joseph Wang**, Ethan Lin, Justin Hsieh, Global UniChip Corp., Taipei, Taiwan

THERMAL AWARE VECTORLESS EM/IR SIGNOFF FOR HIGH SPEED CUSTOM DIGITAL IPS

Ayan Roy Chowdhury, Intel, Karnataka, India

SYSTEM POWER INTEGRITY ANALYSIS: FROM THE PMIC TO THE TRANSISTOR

Shane Stelmach, Texas Instruments, Dallas, TX

STATIC AND FORMAL

Time: 10:30 AM – 12:00 PM

Event Type: Engineering Tracks

Topic Area(s): Front-End Design

Room: 2010, 2nd Floor

Session Chair(s): Vikas Sachdeva (Real Intent Inc)

Static and formal based flows/solutions provide bottom-up verification approach, this helps to find certain class of bugs in the shortest time and help manage efficient distribution of load across all verification technologies. In this session, presenters will share their experiences on applications like data path validation, formal verification at SoC level and CDC (clock domain crossing) verification.

CROSSING THE RISC-V CUSTOMIZATION BARRIER WITH FORMAL

Nicolae Tusinschi, **Salaheddin Hetalani**, Siemens EDA, Munich, Germany; Pascal Gouedo, Dolphin Design, Grenoble, France; Joe Hupcey III, Siemens EDA, Mountain View, CA

A LEAP FORWARD IN ARCHITECTURAL FORMAL CONVERGENCE USING AUTOMATED CASE SPLITTING

Shahid Ikram, Marvell, Boston, MA; Erik Seligman, Cadence Design Systems, Inc., Wichita, KS

DIVIDE, CONQUER, UPSCALE! CONQUERING THE CHALLENGES IN FORMAL FOR SOCS

Ameya Mulye, Analog Devices, Wilmington, MA

FORMAL VERIFICATION: FIRST LINE OF DEFENSE FOR SECURING YOUR HARDWARE FROM ATTACKS

Vedprakash Mishra, Intel, Bengaluru, India; Anshul Jain, Intel, Delhi, India; **Aarti Gupta**, Intel, Cupertino, CA

CONVERGENCE EXPERIMENT: CLOSED LOOP DATA-SENSE QUALIFIER-BASED BUS SYNCHRONIZER TO OVERCOME CONVERGENCE VIOLATIONS IN CLOCK DOMAIN CROSSINGS

Bhargav S, Synopsys, Bangalore, India

FORMAL VERIFICATION OF FLOATING-POINT MATRIX MULTIPLY-ADD DESIGNS

Emiliano Morini, Christopher Poole, Intel, Folsom, CA

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EVERYTHING YOU SHOULD KNOW ABOUT UCIE

Time: 10:30 AM – 12:00 PM

Event Type: Engineering Tracks

Topic Area(s): IP

Room: 2012, 2nd Floor

Session Chair(s): Nelly Feldman (Synopsys)

In his seminal paper that became the basis of Moore's law ("Cramming more components onto integrated circuits" – published in Electronics, Volume 38, Number 8, on April 19, 1965), Gordon Moore also predicted that "It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected." It certainly appears that his prophecy has come true, as we can see that one of the most promising, and successful recent technologies is based on chiplets, where individual dies (often created using different technology nodes) are combined to form an advanced design.

Today we see that leading chip vendors such as Intel and AMD have adopted chiplet-based designs, and chiplet technology is gaining rapid adoption. The popularity of chiplets necessitates an open standard to further enable a chiplet ecosystem. An industry consortium established in early 2022 has been working hard to standardize die-to-die interconnect via the UCle – the Universal Chiplet Interface Express.

In this invited session, you will hear from recognized leaders in the die-to-die interconnect domain as they break down the standard for you.

UNIVERSAL CHIPLLET INTERCONNECT EXPRESS (UCIE)™: AN OPEN INDUSTRY STANDARD DRIVING INNOVATIONS AT THE PACKAGE LEVEL

Debendra Das Sharma, Intel, Santa Clara, CA

SLOWING DOWN OF MOORE'S LAW: HOW TO SCALE PERFORMANCE?

Durgesh Srivastava, NVIDIA, Cupertino, CA

SILICON HEALTH OF UCIE-BASED MULTI-DIE SYSTEMS

Yervant Zorian, Synopsys, Fremont, CA

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AUTODL: AUTOMATED TOOLS FOR FAST DEVELOPMENT OF DEEP LEARNING NETWORKS AND ACCELERATORS

Time: 10:30 AM – 12:00 PM

Event Type: Tutorial

Topic Area(s): AI

Room: 3004, 3rd Floor

Organizer(s): Yingyan (Celine) Yin, Georgia Institute of Technology, Atlanta, GA

Deep neural networks (DNNs) have experienced significant breakthroughs in various artificial intelligence (AI) applications, leading to a growing interest in designing efficient DNNs that can be used on resource-constrained edge devices. One of the most promising techniques for achieving this is hardware-aware Neural Architecture Search (HW-NAS), which automates the process of designing efficient DNN structures for different applications and devices based on specified hardware-cost metrics, such as latency or energy. However, developing optimal HW-NAS solutions is challenging due to the computationally expensive training process and the need for cross-disciplinary knowledge in algorithm, micro-architecture, and device-specific compilation. Additionally, designing DNN accelerators is non-trivial and requires a large team of experts. Research has also shown that optimal DNN accelerators require a joint consideration of network structure, accelerator design, and algorithm-to-hardware mapping, but this direction of jointly designing or searching for all three aspects has only been slightly explored.

The tutorial aims to educate the research community on the challenges of co-searching DNNs and hardware, and to bring together researchers and practitioners interested in automating co-design for deployment in resource-constrained devices. Specifically, we will present our following works addressing the above challenges.

HW-NAS-BENCH

Introduction: HW-NAS-Bench is the first public HW-NAS dataset aiming to democratize HW-NAS research to non-hardware experts, and to facilitate a unified benchmark comprising state-of-the-art NAS search spaces.

Chaojian Li, Georgia Institute of Technology, Atlanta, GA

DNN-CHIP PREDICTOR

Introduction: DNN-Chip Predictor is an analytical tool which accurately predicts various performance metrics of DNN accelerators to help facilitate the fast DNN accelerator design space exploration and optimization before actual ASIC/FPGA implementation. The tool is validated using different DNN models and accelerator designs.

Yang Zhao, Rice University, Atlanta, GA

PRIME

Introduction: Prime is an approach focused on architecting accelerators based on data-driven optimization that only utilizes existing logged data, consisting of accelerator designs and their corresponding performance metrics to architect hardware accelerators without any further hardware simulation. This alleviates the need to run time-consuming simulations and enables reuse of data from past experiments, even when the set of target applications changes and even for unseen but related applications to the training set, in a zero-shot fashion.

Amir Yazdanbakhsh, Google, San Jose, CA

FBNETV5

Introduction: FBNetV5, a NAS framework that can search for DNN networks for a variety of vision tasks with much reduced computational cost and human effort. Specifically, we design 1) a search space that is simple yet inclusive and transferable; 2) a multitask search process that is disentangled with target tasks' training pipeline; and 3) an algorithm to simultaneously search for networks for multiple tasks with a computational cost agnostic to the number of tasks

Bichen Wu, Meta, Santa Clara, CA

AUTO-NBA

Introduction: Auto-NBA is an automated framework that jointly searches for the Networks, Bitwidths, and Accelerators, by efficiently localizing the optimal design within the huge joint design space for each target dataset and accelerator specification. Auto-NBA generated networks and accelerators consistently outperform state-of-the-art designs in terms of search time, task accuracy, and accelerator efficiency.

Yonggan Fu, Yongan Zhang, Rice University, Houston, TX

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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HARDWARE AND SOFTWARE CO-DESIGN FOR EDGE AI

Time: 10:30 AM – 12:00 PM

Event Type: Tutorial

Topic Area(s): AI

Room: 3003, 3rd Floor

Organizer(s): Jana Doppa, Washington State University, Pullman, WA

Many real-world edge applications including self-driving cars, mobile health, robotics, and augmented reality (AR) / virtual reality (VR) are enabled by complex AI algorithms (e.g., deep neural networks). Currently, much of this computation for these applications happen in the cloud, but there are several good reasons to perform the processing on local edge platforms (e.g., smartphones). First, it will increase the accessibility of AI applications to different parts of the world by reducing the dependence on the communication fabric and the cloud infrastructure. Second, many of these applications such as robotics and AR/VR require low latency. We may not be able to achieve their critical real-time requirements without performing the computation directly on the edge platform. Third, for many important applications (e.g., mobile health), privacy and security are important concerns (e.g., medical data). Since edge platforms are constrained by resources (power, computation, and memory), there is a great need for innovative solutions to realize the vision of practically useful Edge AI. This tutorial will address inference and training tasks using different neural networks including CNNs and GNNs for diverse edge applications. The presenters will describe the most-compelling research advances in the design of hardware accelerators using emerging technologies (e.g., ReRAM, monolithic 3D, heterogeneous cores, chiplets); software approaches (e.g., model pruning, quantization of weights, adaptive computation); and various approaches for synergistic co-design to push the Pareto front of energy, performance, accuracy, and privacy.

Presenters: Jana Doppa, Washington State University, Pullman, WA; Umit Ogras, University of Wisconsin, Madison, WI; Priyadarshini Panda, Yale University, New Haven, CT

MACHINE LEARNING BASED ANALYTICS TOWARDS AUTOMATED COMPUTING SYSTEM MANAGEMENT

Time: 10:30 AM – 12:00 PM

Event Type: Tutorial

Topic Area(s): AI, Cloud

Room: 3006, 3rd Floor

Organizer(s): Burak Aksar, Boston University, Boston, MA

Machine learning (ML) has been heavily integrated into many application areas; however, computer system management relies heavily on expert-generated, often fragile methods with limited automation. This tutorial aims to familiarize the audience with ML-based telemetry analytics for computing systems to improve system performance, resilience, and power efficiency. Computer systems are increasingly built with power constraints (from embedded systems to building exascale high-performance computing systems), leading to increasing levels of resource sharing, contention, and unpredictable performance due to “anomalies.” Such anomalies resulting from software bugs, intermittent hardware or system problems, or contention of shared resources (memory, CPU, network, etc.) cause inefficiency. A common way to assess system performance and identify the root causes of problems is through gathering and inspecting telemetry data, which includes time series information on how various subsystems in a computer system are utilized. Today, any computer system can easily support a collection of telemetry and log data from hundreds (or often thousands) of hardware and software sensors. However, manual analysis is impractical given the billions of data points collected each day. Given the severe limitations of manual analysis, ML is gaining popularity as a promising method to automate performance analytics. Additionally, computer system telemetry analytics is a difficult application area for ML with many unsolved problems since labeled training data is sparse, while unlabeled data can reach up to terabytes per day.

This tutorial aims to demonstrate the lessons learned through recent ML-based computer system analytics methods that have been tested with real-world data and real systems. The tutorial begins by giving a general overview of analytics using telemetry data and demonstrating the promise of ML-based methods compared to currently used techniques, which frequently rely on heuristics with heavy human involvement. The tutorial also intends to introduce a multitude of ML-based methods capable of detecting performance anomalies as well as their underlying causes or recognizing apps that run on a computer system. Participants will also have the opportunity to participate in hands-on activities through the open-source analytics frameworks designed by the speakers’ teams. Upon completing this tutorial, participants will have a broader knowledge of the challenges, opportunities, and skills necessary to use ML-based methods to solve complex computer system problems.

Presenters: Ayse Coskun, Burak Aksar, Efe Sencan, Boston University, Boston, MA; Ben Schwaller, Jim Brandt, Sandia National Laboratories, Albuquerque, NM

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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REINFORCING CIRCUIT AND LAYOUT SYNTHESIS

Time: 10:30 AM – 12:00 PM

Event Type: Tutorial

Topic Area(s): AI, EDA

Room: 3008, 3rd Floor

Organizer(s): Shubham Rai, Technische Universität Dresden, Germany

Circuit and layout synthesis are important steps in design flows for building integrated circuits (ICs). However, conventionally, many steps, from digital logic to analog layout, are either governed by various heuristics-based optimizations or implemented by humans. Designers may have to rely heavily on their knowledge and experience to achieve design closure. Reinforcement learning (RL) has lately acquired attention to replacing human expertise in chip design. An optimization problem can be converted into a control problem in MDP, where design optimization targets are translated into environmental rewards, and design variables are converted into environmental actions. An RL agent can learn an effective policy in selecting the actions based on the current environmental state.

This particular tutorial aims to present the recent developments in applying RL in both digital and analog circuit synthesis. We demonstrate the learning-driven synthesis algorithms that give more consistent and efficient results than handcrafted classical approaches. Within this tutorial, there are there talks that present the state-of-the-art learning techniques used in digital and analog synthesis. Major challenges will also be discussed to motivate future research directions.

Presenters: Shubham Rai, Technische Universität Dresden, Germany; Cunxi Yu, University of Utah, Salt Lake City, UT; Huigang Liao, Cadence Design Systems, Inc., San Francisco, CA; Keren Zhu, The University of Texas at Austin, TX

SCALABLE HARDWARE SECURITY VERIFICATION USING INFORMATION FLOW TRACKING

Time: 10:30 AM – 12:00 PM

Event Type: Tutorial

Topic Area(s): Security

Room: 3002, 3rd Floor

Organizer(s): Jason Oberg, Cycuity, San Francisco, CA

Security verification is a growing and crucial area for the commercial semiconductor market. Organizations are continuing to grow their product security teams and build verification infrastructure that can help identify and mitigate security weaknesses in hardware designs. With the growing complexity of modern SoCs, with gate counts often exceeding 1 billion, solutions that can effectively verify the lack of security weaknesses at a large scale are becoming increasingly important. This fact is compounded by the complexity of software that powers these SoCs, further complicating the ability to verify security.

Information flow tracking techniques have been around for decades but have only recently emerged as a powerful solution for helping identify security weaknesses in modern SoCs at scale. Recent technical advances in these approaches have made the ability to deploy these techniques on commercial-grade SoC designs a reality with improved optimizations and analysis techniques.

The tutorial starts with Ryan Kastner giving a background on information flow tracking (IFT), diving into its technical foundations, and describing how it developed into an invaluable verification tool to detect and prevent hardware design weaknesses. Next, Cynthia Sturton will lay out the theoretical foundations behind the types of properties used to describe information-flow, describe the fundamental difference between safety properties and hyperproperties, and explain how information-flow properties can be generated using information flow tracking. Then, Jason Oberg will overview commercial hardware security IFT-based verification tools and provide key insights on how to best use them to uncover security vulnerabilities in large hardware designs. Last, Jagadish Nayak will conduct live demonstrations using the Cycuity Radix IFT verification tools on OpenTitan – an open-source, commercial-grade hardware root of trust. He will enumerate key OpenTitan design assets using hardware Common Weakness Enumerations (CWEs), analyze potential weaknesses and vulnerabilities using the Radix tools, provide a fix for the uncovered vulnerabilities, and verify that the patched hardware redesign removes the vulnerabilities. The vulnerabilities were previously unknown, and the mitigations were submitted to the OpenTitan repository and subsequently accepted.

Presenters: Ryan Kastner, University of California, San Diego, CA; Jason Oberg, Cycuity, San Francisco, CA; Jagadish Nayak, Cycuity, San Diego, CA; Cynthia Sturton, University of North Carolina, Chapel Hill, NC

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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BUILDING THE METAVERSE: AUGMENTED REALITY APPLICATIONS AND INTEGRATED CIRCUITS CHALLENGES

Time: 11:30 AM – 12:30 PM

Event Type: TechTalk

Topic Area(s): Design

Room: DAC Pavilion, Level 2 Exhibit Hall

Augmented reality is a set of technologies that will fundamentally change the way we interact with our environment. It represents a merging of the physical and the digital worlds into a rich, context aware and accessible user interface delivered through a socially acceptable form factor such as eyeglasses. One of the biggest challenges in realizing a comprehensive AR experience are the performance and form factor requiring new custom silicon. Innovations are mandatory to manage power consumption constraints and ensure both adequate battery life and a physically comfortable thermal envelope. This presentation reviews Augmented Reality and Virtual Reality applications and Silicon challenges.

Presenter: Edith Beigne, Meta, Menlo Park, CA

MICROELECTRONICS SECURITY: A GROWING NATIONAL IMPERATIVE

Time: 1:00 PM – 1:45 PM

Event Type: SKYTalk

Topic Area(s): Security

Room: DAC Pavilion, Level 2 Exhibit Hall

The microelectronics industry continues to play a fundamental role in our nation's economic and national security, and technological standing. The recent CHIPS Act and ongoing Department of Defense initiatives such as the Rapid Assured Microelectronics Prototypes (RAMP) program, underscore the government's commitment to accelerating the nation's rapid pace of microelectronics innovation and enable U.S. development of the very best in circuit design, manufacturing, and packaging. But how are we ensuring security across the microelectronics supply chain?

Our guest speaker, Dr. Devanand Shenoy will provide insights into how a number of DoD and commercial initiatives and investments are strengthening our microelectronics security posture across the development and deployment of leading-edge microelectronics technologies. Learn more about how these programs present opportunities for the Design Automation Conference (DAC) community to participate in the strengthening of our microelectronics cybersecurity readiness.

Presenters: Devanand Shenoy, U.S. Department of Defense, Washington, DC; Andreas Kuehlmann, Cycuity, San Francisco, CA

THE GOOD, BAD AND CLOUDY

Time: 1:00 PM – 1:45 PM

Event Type: Transformative Technologies Theater

Topic Area(s): Cloud, EDA

Room: Transformative Technologies Theater, Level 1 Exhibit Hall

Over the past couple of years, chip design on cloud has grown considerably. It is happening and is here to stay. From pay-per-use licensing, to single click environment creation to reference architectures – chip design democratization path seems to be set. But all is not done – much more remains to be done. Hear from a panel of users and vendors on what works (and what doesn't) and what are some key challenges remaining to be addressed.

Moderator: Ann Mutschler, Semiconductor Engineering, Louisville, KY

Presenters: Rob Aitken, Synopsys, San Jose, CA; Mahesh Turaga, Cadence Design Systems, Inc., San Jose, CA; Craig Johnson, Siemens EDA, San Francisco, CA; Richard Ho, Lightmatter, Mountain View, CA; Phil Steinke, AMD

IMPLEMENTATION CHALLENGES IN COMPLEX 3D/HETEROGENEOUS ARCHITECTURES

Time: 1:30 PM – 3:00 PM

Event Type: Engineering Tracks

Topic Area(s): Back-End Design

Room: 2008, Level 2

Organizer/Moderator: Sabya Das, Synopsys, San Francisco, CA

As the design architectures get more complex with 2.5/3-D and heterogeneous aspects, continuous innovation is needed in both hardware space and the EDA software domain. This session focuses on various implementation challenges. The first talk is a discussion about the foundational EDA challenges in enabling 3D-ICs, including the system design and optimization of 3DIC architecture, multi-die co-design and co-optimization, and management of scale complexity. The second talk describes the physical design flows in the multi-die, adaptive compute acceleration platform for partially reconfigurable fabric. A combination of this flow and the architecture is capable of delivering high performance. The final talk is about the latest competitive situation between two power-delivery bonding technologies for 3D heterogeneous integration.

Presenters: Deming Chen, University of Illinois at Urbana-Champaign, Urbana, IL; Amit Gupta, AMD, Los Altos, CA; Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

DRAGGING DEBUG INTO A NEW ERA

Time: 1:30 PM – 3:00 PM

Event Type: Engineering Tracks

Topic Area(s): Front-End Design

Room: 2010, 2nd Floor

Session Chair(s): Dave Rich (Siemens EDA)

The most time and effort consuming part of our verification process remains debugging, no matter if it is for finding functional or performance bugs or localizing defects. Hence, any change in the efficiency of this process will significantly improve the overall efficiency. Efforts using advanced data analytics and ML/AI have started to chip off piece by piece from this manual work and is showcasing the importance of methodical data collection. This set of presentations is meant to provide a look at some suggested directions that is dragging (or, really, accelerating) debug into a new era.

Presenters: Andrew Ross, AMD, Boylston, MA; Eric Harris, Arm Ltd., Austin, TX; Alan Pippin, Hewlett Packard Enterprise, Palo Alto, CA

ADVANCED FRONT-END VERIFICATION METHODOLOGIES FOR LEADING-EDGE IP

Time: 1:30 PM – 3:00 PM

Event Type: Engineering Tracks

Topic Area(s): IP

Room: 2012, 2nd Floor

Session Chair(s): Vidyasagar Ganesan (AMD)

Verification, from requirements to proper test benches, often is the first critical milestone for IP development. This session will discuss the fundamental challenges of verification, starting with requirements management throughout the flow, power verification aspects identifying peak power windows and power and timing aspects in automotive, ML-based methodologies, IP library validation, and standards impacting RISC V verification.

REQUIREMENTS MANAGEMENT FLOW ON DIGITAL PROJECTS WITH REQTRACKER

Alessandro Iannuzzi, Antonino Russo, STMicroelectronics, Milano, Italy; Huqing Zheng, STMicroelectronics, San Francisco, CA

IMPROVED PEAK POWER INTERVAL DETECTION USING THE SLIDING WINDOW POWER PROFILE (SWPP)

Saebit Jeong, Woojoo Kim, Kunhyuk Kang, Samsung Electronics, Hwaseong, South Korea; Manish Kumar, Vishnu Kanwar, Vishal Kashyap, Siemens EDA, Noida, India; Jinsuk Youn, BK Yoon, Siemens EDA, Seoul, South Korea

SECURITY, TIMING SYNCHRONIZATION, AND POWER SAVING FOR AUTOMOTIVE ETHERNET: FUNCTIONAL VERIFICATION CHALLENGES AND ITS SOLUTIONS

Shubham Agrawal, Cadence Design Systems, Inc., San Jose, CA; **Krunal Amrutbhai Patel**, Cadence Design Systems, Inc., Gujarat, India

ML-BASED HIGH SIGMA VERIFICATION METHODOLOGY

Kwonchil Kang, **Kihoon Kim**, Samsung Electronics, Hwaseong, South Korea; **Sungyoung Lee**, Siemens EDA, Seoul, South Korea

COMPREHENSIVE VALIDATION SOLUTION FOR SILICON IP&LIBRARY

Lippika Parwani, STMicroelectronics, Greater Noida, India; Jean-Arnaud Francois, STMicroelectronics, Crolles, France; Siddharth Ravikumar, Siemens EDA, Walnut Creek, CA; Wei Tan, Siemens EDA, Fremont, CA; **Anil-Kumar Dwivedi**, STMicroelectronics, Delhi, India

OPEN STANDARDS AND METHODOLOGIES FOR RISC-V VERIFICATION TESTBENCHES

Aimee Sutton, Imperas, Ottawa, Canada; Lee Moore, Simon Davidmann, Kevin McDermott, Imperas, Thame, United Kingdom

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

A JOURNEY TO OPTICAL COMPUTING: FROM PHYSICS FUNDAMENTALS TO HARDWARE-SOFTWARE CO-DESIGN, AUTOMATION, AND APPLICATION

Time: 1:30 PM – 5:00 PM

Event Type: Tutorial

Topic Area(s): AI

Room: 3003, 3rd Floor

Organizer(s): Jiaqi Gu, The University of Texas at Austin, TX;

In the post-Moore era, conventional computing solutions of digital electronics have become a limiting factor in certain domains, most notably intelligent information processing. The proliferation of big data and artificial intelligence (AI) has motivated the investigation of next-generation computing platforms to support low-latency, energy-efficient machine intelligence. With the advances in device, manufacturing, and integration technology, optics/photonics has attracted increasing attention in recent years and is considered to have great potential in key areas of communication, interconnects, sensing, and computing. Due to the ultra-fast speed and high parallelism of optics, computing platforms based on optical interconnects and processing units can make transformative impacts in important use domains, e.g., future datacenters, automotive, smart sensing, and intelligent edge. In recent years, efforts have been made to facilitate the design automation stack of optical computing platforms and push forward the realization and practical application of next-generation optical processors. However, as the complexity of the heterogeneous mixed-signal computing platform escalates, significant design and optimization challenges need to be tackled. In order to have a scalable design closure and unleash the full power of optics, two critical threads need synergistic advancement along this journey, i.e., cross-layer co-design and electronic-photonics design automation.

In this tutorial, we will guide the interested audience on a journey toward next-generation optical processing platforms with a comprehensive introduction to the literature, co-design & automation technologies, hardware implementation, applications, as well as hands-on demos of optical AI computing. We separate the tutorial into four talks covering integrated photonic computing, optical networks-on-chip and robustness analysis, synthesis for field-programmable photonic arrays (FPPAs), and diffractive optical neural networks (DONNs).

Presenters: Jiaqi Gu, Chenghao Feng, Hanqing Zhu, Ray T. Chen, The University of Texas at Austin, TX; Ulf Schlichtmann, Technische Universität München; Zhengqi Gao, Duane Boning, Massachusetts Institute of Technology, Cambridge, MA; Yingjie Li, Cunxi Yu, University of Utah, Salt Lake City, UT

SIDE-CHANNEL ANALYSIS: FROM CONCEPTS TO SIMULATION AND SILICON VALIDATION

Time: 1:30 PM – 5:00 PM

Event Type: Tutorial

Topic Area(s): Security

Room: 3002, 3rd Floor

Organizer(s): Gang Qu, University of Maryland, Imperial College London, College Park, MD; Makoto Nagata, University of Kobe, Japan; Lang Lin, Ansys, Cupertino, CA

Since the report of simple and differential power analysis in the late 1990's, side-channel analysis (SCA) has been one of the most important and well-studied topics in hardware security. In this tutorial, we will share our insights and experience on SCA by a combination of presentations, embedded demos, and an interactive panel discussion. The three speakers are from academia and industry with rich experience and solid tracking record on hardware security research and practice.

We will start the tutorial with a comprehensive introduction of SCA, including the popular side channels that have been exploited by attackers, common countermeasures, and the simulation based SCA with commercial EDA tools at gate level. Then we will present industry proven flows for fast and effective presilicon side channel leakage analysis (SCLA) with focus on physical level power and electromagnetic (EM) side channels. Next, we elaborate how to perform on-chip and in-system side-channel leakage measurements and assessments with system-level assembly options on crypto silicon chips with the help of embedded on-chip noise monitor circuits. We will conclude the presentations with some forward-looking discussion on emerging topics such as SCA for security, SCA in AI and machine learning (ML), and presilicon SCLA assisted by AI/ML. Short video clips will be embedded in the presentation to showcase SCA by simulation and silicon measurement.

No prior knowledge is required to attend this tutorial. The audience is expected to learn the foundations and state-of-the-arts in SCA with some hands-on skills. The total length of the tutorial is 180 minutes, including a 10-minute break. The tentative agenda of the tutorial is as follows:

1. Welcome and introduction (5 minutes)
2. Foundations of side-channel analysis (40 minutes. Common source of side channel leakage, principle and examples of side-channel attacks, and existing mitigation methods.)
3. Simulation-based pre-silicon fast side-channel leakage analysis (40 minutes. Full-stack presilicon simulation principles and fast leakage analysis on power and electromagnetic side channels with industry proven tools and flows)
4. Break (10 minutes)
5. On-chip and in-system side-channel leakage measurements and assessments (40 minutes. Onchip power side channel leakage measurements, in-system electromagnetic side channel leakage measurements, and fault-injection measurements)
6. Demos and Panel (40 minutes. Simulation-based methods and on-chip monitoring for the detection of side channel vulnerabilities.)
7. Conclusion (5 minutes)

Presenters: Gang Qu, University of Maryland, Imperial College London, College Park, MD; Makoto Nagata, University of Kobe, Kobe, Japan; Lang Lin, Ansys, San Jose, CA

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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THE ART OF BUILDING AND ATTACKING SECURE SYSTEMS

Time: 1:30 PM – 5:00 PM

Event Type: Tutorial

Topic Area(s): RISC-V, Security

Room: 3004, 3rd Floor

Organizer(s): Jeyavijayan Rajendran, Texas A&M University, College Station, TX

Hardware is at the heart of computing systems. For decades, software was considered error-prone and vulnerable. However, recent years have seen a rise in attacks exploiting hardware bugs. To alleviate the increasing challenges in hardware, it is vital to raise hardware security awareness among the next generation of security engineers and researchers. In this course, Hack@HAT 101, we introduce software-exploitable hardware vulnerabilities like privilege escalation, information leakage, and denial of service (DoS), and hardware verification techniques such as directed random regression, hardware fuzzing, and formal techniques.

Participants will get a real-world open-source RISC-V based system-on-chip (SoC) with vulnerabilities we inserted in collaboration with security researchers from Intel, spanning various hardware Common Weakness Enumerations (CWEs). We will provide the tools and documentation required to run the SoC. With our assistance, participants will get hands-on, capture-the-flag competition-style experience by working in teams to identify the vulnerabilities in this SoC. We will also explore how recent advances in AI-driven automatic code synthesis (e.g., GitHub Copilot) intersect with this domain, with specific hands-on examples illustrating how these AI models can both introduce security-relevant bugs as well as later patch them. The examples will include simple examples (register lock bits) and more complex procedures (bus translation of security privileges).

Presenters: Jeyavijayan Rajendran, Texas A&M University, College Station, TX; Ahmad-Reza Sadeghi, Technische Universität Darmstadt, Hessen, Germany; Ramesh Karri, New York University, New York City, NY; Tuba Yavuz, University of Florida, Gainesville, FL

TIMING CHALLENGES AT ADVANCED TECHNOLOGY NODES AND ACCELERATION BY HETEROGENEOUS PROGRAMMING AND MACHINE LEARNING

Time: 1:30 PM – 5:00 PM

Event Type: Tutorial

Topic Area(s): AI, EDA

Room: 3008, 3rd Floor

Organizer(s): Iris Hui-Ru Jiang, National Taiwan University, Taipei, Taiwan

Timing analysis is essential to every step in the circuit design flow. Due to its high computational complexity, timing analysis has become the bottleneck of the entire design flow. Timing analysis, verifying the timing performance of a design under worst-case conditions, is of particular importance to design closure. In this tutorial, we start with timing challenges and considerations at advanced technology nodes from the foundry's perspective, followed by acceleration techniques, including heterogeneous programming and machine learning for expediting timing analysis and optimization.

Presenters: Pei-Yu Lee, MediaTek, Hsinchu, Taiwan; Florin Dartu, Kevin Chen, TSMC, Hsinchu, Taiwan; Tsung-Wei Huang, University of Utah, Salt Lake City, UT; Iris Hui-Ru Jiang, National Taiwan University, Taipei, Taiwan; Yibo Lin, Peking University, Beijing, China

VIRTUAL AND SCENARIO-BASED TESTING OF AUTONOMOUS SYSTEMS

Time: 1:30 PM – 3:00 PM

Event Type: Tutorial

Topic Area(s): Autonomous Systems

Room: 3006, 3rd Floor

Organizer(s): Wenchao Li, Boston University, Boston, MA;

Due to the sheer complexity and variability in the operating environment, how to systematically test autonomous systems to gather enough confidence on the safety and reliability of their operation remains an open challenge. Virtual testing is a widely adopted methodology for complementing expensive and limited field or road tests. This session features two short tutorials presenting techniques, tools and practices for conducting scenario-based testing of autonomous systems in virtual environments.

Presenters: BaekGyu Kim, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Daniel Fremont, University of California, Santa Cruz, CA

Research Sessions

Special Session

Panel

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Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

FAAS – HYPED UP NEW ACRONYM OR A WAY TO LEVEL THE SIMULATION PLAYING FIELD? THE OPPORTUNITIES AND CHALLENGES OF FAAS (FUNCTION AS A SERVICE) FOR ACCELERATING SIMULATION AND ANALYSIS.

Time: 2:00 PM – 2:45 PM

Event Type: DAC Pavilion Panel

Topic Area(s): Cloud, EDA

Room: DAC Pavilion, Level 2 Exhibit Hall

SaaS (Software as a Service) and HPC (High Performance Computing) are now common terms in the design community. However, an emerging concept is that of FaaS (Function as a Service). FaaS holds promise for drastically improving circuit, electromagnetic, and signal integrity simulation performance while enabling rapid analysis and design exploration. Yet adoption of FaaS in semiconductor, printed circuit and RF design roles has been slow, and many organizations have questions and concerns about its feasibility, security, or are simply unaware of its existence.

The design community traditionally invests in large server infrastructure when there's a need to accelerate circuit simulation, SI, and electromagnetic modeling. In addition to the heavy cost of hardware and power consumption, configuration management and maintenance costs can often outweigh the benefits of data security and optimization. Moreover, companies that deploy HPC internally become committed to running on an "upgrade-or-die" hamster wheel.

FaaS is an attractive alternative because it allows vendors to execute small pieces of code on the network edge, making the codebase more scalable without having to spend resources on maintaining the back-end. With FaaS, provisioning resources takes a few seconds rather than minutes or hours and is not limited to a particular language or resource. FaaS is fast becoming a method of choice for accelerating compute intensive applications that retain a desktop environment such as EDA tools. This approach, known as "microservices," is appealing because it also means vendors can easily make incremental improvements and new features to back-end code without costly desktop deployments.

With traditional SaaS HPC, when a function has not been called for a period of time, the provider shuts it down to save energy and avoid over-provisioning. The next time a user runs an application that calls that function, the provider spins it up fresh and starts hosting that function again, which takes time. This startup latency, known as a "cold start," is one of several bottlenecks to adoption.

In contrast, FaaS worker node functions spin up at the edge in a very short amount of time. As more such drawbacks are addressed and the popularity of edge computing grows, we can expect FaaS adoption to grow in the EDA and Test/Measurement landscape. But will it?

FaaS decouples the user from back-end computation in a way that offers unprecedented scalability, but how is it different from the current generation of EDA HPC cloud acceleration options? And how can it be leveraged to save time and cost during development? Why would one choose FaaS over owned internal HPC resources?

This panel will bring together experts from semiconductor design, EDA software, and electronic product integration to discuss the opportunities and the drawbacks – perceived and real – of using FaaS for acceleration of design and simulation workflows. The diverse group on the panel will ensure a broad set of interests and viewpoints are represented.

Moderator: Ben Jordan, JordanDSP, Escondido, CA

Panelists: Rajath Narasimha, Keysight, San Francisco, CA; Ryan Magruder, Rescale, Mountain View, CA; Yi Cao, Meta Reality Labs; Kenneth Hill, Eviden

COOLEY'S DAC TROUBLEMAKER PANEL

Time: 3:00 PM – 4:00 PM

Topic Area(s): EDA, Design

Room: Room 3016, Moscone West, Level 3, above DAC Exhibit Hall

Come watch the EDA troublemakers answer the edgy, user-submitted questions about this year's most controversial issues! It's an old-style open Q&A from the days before corporate marketing took over every aspect of EDA company images.

Moderator: John Cooley, Deepchip

Panelists: Joe Sawicki, Siemens EDA; Tom Beckley, Cadence Design Systems, Inc.; Joe Costello, Executive Chairman at Metrics, Kwikbit, Arrikto, Acromove; Dean Drako, IC Manage; Prakash Narain, Real Intent; Surprise Guest Panelist

Research
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DAC Pavilion Panel;
Analyst Review

TechTalk
SKYTalk

Keynotes and
Visionary Talks

Engineering
Track

DESIGN AUTOMATION FOR QUANTUM COMPUTING

Time: 3:00 PM – 3:45 PM

Event Type: Tech Talk

Topic Area(s): Design

Room: DAC Pavilion, Level 2 Exhibit Hall

Quantum computers have the potential to solve certain tasks that would take millennia to complete even with the fastest (conventional) supercomputer. Numerous quantum computing applications with a near-term perspective (e.g., for finance, chemistry, machine learning, optimization) and with a long-term perspective (i.e., cryptography, database search) are currently investigated.

The Design Automation Community needs to be ready for this! In fact, due to the radically different computational primitives, seemingly simple tasks in the design of corresponding computers and algorithms get substantially harder for quantum computing compared to conventional circuits and systems. This affects how we currently conduct design automation for quantum computing—or how we do not. In fact, established programming languages, synthesizers, design tools, test, or verification schemes do not work for quantum computers anymore. In many aspects, considering the design for quantum computers, we are back at square one. And this may lead to a situation where we may have quantum computers but no proper (automatic) methods that aid us in using their potential!

In this talk, we discuss how design automation can help and how we can get design automation experts excited for this emerging technology. To this end, we report from our long-standing expertise in this domain and our experiences on bridging the quantum computing and the EDA community. We illustrate that quantum computing is no “rocket science” and, using proper models and abstractions, design automation can make a huge difference. This is showcased by several methods and software tools which have been developed in the past years with design automation in mind. Finally, the integration of these methods, tools, and mindsets into entire ecosystems (covering the entire flow from applications to eventual realization) is presented.

About the speaker: Robert Wille is Full and Distinguished Professor at the Technical University of Munich, Germany, and Chief Scientific Officer at the Software Competence Center Hagenberg GmbH, Austria (a technology transfer company with more than 100 employees). For more than 15 years, he is working on topics in the domain of quantum computing and successfully established design automation concepts in this domain. The impact of his work is reflected by numerous awards such as Best Paper Awards, e.g., at TCAD and ICCAD, a DAC Under-40 Innovator Award, a Google Research Award, etc., collaborations with industrial partners in this domain (such as IBM, Google, AQT, etc.), as well as his involvement in prestigious projects and initiatives, e.g., within the scheme of an ERC Consolidator Grant or the comprehensive quantum computing initiative of the Munich Quantum Valley.

Presenter: Robert Wille, Technische Universität München, SCCH GmbH, Munich, Germany

AI ON THE EDGE! CHALLENGES AND SOLUTIONS FOR EDGE AI PRODUCTS

Time: 3:30 PM – 5:00 PM

Event Type: Engineering Tracks

Topic Area(s): Embedded Systems and Software

Room: 2008, Level 2

Organizer: Moshe Zalcberg, Petach Tikva, Israel

Artificial Intelligence (AI) is everywhere, but continuously moving from the datacenter core to the edge: cars, surveillance cameras, machines, home appliances, wearables, health equipment – everything is becoming smart, with the addition of AI. But “AI on the Edge” adds some interesting engineering challenges and different trade-offs for form-factor, power envelope, cost and performance.

Moreover, multiple technologies are being proposed to address these challenges: different architectures of hardware/software, analog/digital, logic/memory, etc.

This session will review some of the different paradigms innovative startup companies are working on and the possible solutions to those challenges.

Moderator: Raul Camposano, Silicon Catalyst, Santa Clara, CA

Presenters: Steve Roddy, Quadric, Livermore, CA; Alexander Timofeev, POLYN Technology, Haifa, Israel; Mirko Prezioso, Mentium Technologies, Santa Barbara, CA; Peter Suma, Applied Brain Research, Aurora, Canada

Research Sessions

Special Session

Panel

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Keynotes and Visionary Talks

Engineering Track

ADAPTING TO A NEW ERA IN FRONT-END DESIGN AND VERIFICATION OF POWER

Time: 3:30 PM – 5:00 PM

Event Type: Engineering Tracks

Topic Area(s): Front-End Design

Room: 2010, 2nd Floor

Session Chair(s): Homayoon Akhiani (NVIDIA)

NODE BASED CLOCK GATING: REDUCING NOC POWER IN LOW BANDWIDTH SCENARIO

Kyurae Lee, Samsung Electronics, Hwaseong, South Korea; **Wooil Kim**, University of Illinois at Urbana-Champaign, Urbana, IL

LOW POWER AND AREA EFFICIENT 64 BIT VEDIC MULTIPLIER DESIGN FOR HIGH SPEED OPERATION IN ASIC-DSP APPLICATIONS.

Pooja Krishnamurthy, Silicon Interfaces, Mumbai, India; **Priyanka Gharat**, Sastry Puranapanda, Darshan Sarode, Silicon Interfaces, Maharashtra, India

POWER INTENT AUTOMATION FOR ULTRA LOW POWER MIXED-SIGNAL SOC

Sai Sudarsan Chitrapu, BITS Pilani, Pilani, India; **Ruchi Shankar**, Ankitha M, Texas Instruments, Ankitha M, Penchal Kumar Gajula, Lakshmanan Balasubramanian, Gaurav Kumar, Texas Instruments, Bangalore, India

LOW POWER DAC SUB-SYSTEM FOR DIGITAL BEAM FORMING CHIP

Ankur Bal, **Rupesh Singh**, STMicroelectronics, Noida, India

FULL SOC POWER ANALYSIS AND ESTIMATION WITH END-USER SOFTWARE EARLY IN THE DESIGN CYCLE

Jongwoo Ryu, Jinsuk Youn, Woojoo Kim, Kunhyuk Kang, Samsung Electronics, Hwaseong, South Korea; **Amir Attarha**, Siemens EDA, Frisco, TX; **Justin Lee**, BK Yoon, Siemens EDA, Seoul, South Korea

UNIQUE METRIC DRIVEN VECTOR QUALIFICATION AND RANKING FOR PEAK POWER COVERAGE

Seunghyeon Park, Jinsuk Youn, Wojoo Kim, Kunhyuk Kang, Samsung Electronics, Hwaseong, South Korea

ADVANCED VERIFICATION METHODOLOGIES FOR LEADING-EDGE IP – MEMORIES, FPUS, AND SECURITY

Time: 3:30 PM – 5:00 PM

Event Type: Engineering Tracks

Topic Area(s): IP

Room: 2012, 2nd Floor

Session Chair(s): Himanshu Sanghavi (Meta)

SHIFT LEFT DETECTION OF LOGIC EQUIVALENCE ABORT POINTS VIA RTL LINTER

Amit Goldie, Himanshu Kathuria, Synopsys, Noida, India; **Suresh Babu Barla**, Synopsys, San Jose, CA; **Makarand Patil**, Synopsys, Pune, India; **Paras Mal Jain**, Synopsys; **Rohit Kumar Ohlayan**, Synopsys

DIGITAL DESIGN FLOW FOR AREA-CONSTRAINED IPS USING CUSTOM NON-STANDARD IEEE-754 FORMAT

Marco Castellano, STMicroelectronics, Pavia, Italy; **Marco Leo**, STMicroelectronics, Milano, Italy

DYNAMIC CDC(CLOCK DOMAIN CROSSING) FOR MEMORY DESIGN

Inryoul Lee, Samsung Electronics, Hwaseong, South Korea

A ROBUST FRAMEWORK FOR HIGH SPEED LINK VERIFICATION WITH A PROFICIENT WAY TO CLOSE THE FUNCTIONAL COVERAGE

Piyush Tankwal, **Arnab Ghosh**, **Piyush Agnihotri**, **Mukesh Gandhi**, **Parag S. Lonkar**, Samsung R&D (SSIR), Bangalore, India

SECURITY VERIFICATION OF HARDWARE SYSTEM USING FORMAL

Igrajo Lee Anthony, Analog Devices, General Trias, Philippines

PBR BANK CONFLICT AVOIDANCE SCHEDULING TO ENHANCE DRAM BANK UTILIZATION

Hyunjoon Kang, Heeju Kim, Wooil Kim, Manwhae Jo, Taehun Kim, Samsung Electronics, Hwaseong, South Korea

ASK ME ANYTHING WITH SEAN JENSEN-GREY

Time: 3:30 PM – 4:15 PM

Event Type: Transformative Technologies Theater

Topic Area(s): Cloud, EDA

Room: Transformative Technologies Theater, Level 1 Exhibit Hall

Join Sean Jensen-Grey for an interactive session, where Sean will answer questions relevant to chip design on cloud. Attend this AMA session on using cloud computing to scale EDA workloads. We'll discuss the benefits of on-demand access to computing resources, the challenges of deploying EDA tools on the cloud, best practices for optimizing EDA workloads in the cloud, and emerging trends in this space.

Questions that will be examined:

- What are the benefits of using cloud computing for EDA workloads, and how does it help to scale them?
- What are the challenges associated with deploying EDA tools on the cloud, and how can they be overcome?
- What are some of the key considerations when selecting a cloud provider for EDA workloads?
- How can organizations ensure the security and privacy of their EDA workloads in the cloud?
- What are some of the best practices for optimizing EDA workloads in the cloud?
- How can cloud computing be used to enhance collaboration and productivity among EDA teams?
- What are some of the cost considerations associated with using cloud computing for EDA workloads, and how can organizations optimize their costs?
- What are some of the emerging trends in cloud computing for EDA workloads, and how can organizations stay ahead of the curve?
- How does the adoption of cloud computing for EDA workloads impact the overall design process, and what are the potential benefits for design teams?

Presenter: Sean Jensen-Grey, Google, Mountain View, CA

ARCHITECTURES AND MACHINE LEARNING MODELS FOR HIGH-ASSURANCE AUTONOMOUS SYSTEMS

Time: 3:30 PM – 5:00 PM

Event Type: Tutorial

Topic Area(s): Autonomous Systems

Room: 3006, 3rd Floor

Organizer(s): Wenchao Li, Boston University, Boston, MA

The use of data-driven and machine learning components present significant challenges in the development of high-assurance autonomous systems. This session features two short tutorials presenting methodologies, techniques and tools for addressing these challenges, ranging from requirements, through functional architectures, to analysis techniques that can enhance the resilience, interpretability and ultimately trustworthiness of such autonomous systems.

Presenters: Alessandro Pinto, NASA Jet Propulsion Laboratory, Berkeley, CA; Susmit Jha, SRI International, Menlo Park, CA

MONDAY ENGINEERING TRACK POSTER RECEPTION

Time: 5:00 PM – 6:00 PM

Event Type: Engineering Track Poster

Room: Level 2 Exhibit Hall

A COMPREHENSIVE THERMAL SOLUTION IN ADVANCED LARGE SCALE 3DIC DESIGN

Keqing Ouyang, Ping Ding, Junjie Chen, Guohua Zhou, Haodong Lei, Sanechips Technology Co., Ltd, Shenzhen, China; Li Zou, Ansys, Austin, TX; Chang Zhao, Ansys, Shanghai, China

A METHOD TO PLAN & GENERATE IO RING BASED ON CSV SPECIFICATIONS

Akshita Bansal, Hitesh Marwah, Cadence Design Systems, Inc., Noida, India; Atul Bhargava, STMicroelectronics, Greater Noida, India; Vishesh Kumar, Cadence Design Systems, Inc., Bangalore, India; Rajeev Singh, Manvi Dhawan, STMicroelectronics, Delhi, India

A STRUCTURED WAY OF COMMUNICATION IN LAYOUT DESIGN FLOW THROUGH VIRTUOSO DESIGN INTENT

Priya Meharde, Aditya Sharma, Atul Bhargava, STMicroelectronics, Noida, India; Anil Nagendra, STMicroelectronics, Bangalore, India; Priyanshi Shukla, Cadence Design Systems, Inc., Kanpur Nagar, India

ADVANCED TRANSCIEVER COMPONENTS FOR ROBUST HANDLING OF SIGNAL NOISE AND LOSS

Danfeng Xu, Arnav Shah, Gary Kwan, eTopus Technology Inc., Palo Alto, CA; Pradeep Thiagarajan, Siemens EDA, Raleigh, NC

AGGRESSOR AWARE DESIGN FOR BETTER IRDROP RESULTS

Vlad Berlin, Eddie Reizin, Retym, Center District, Israel; Boris Shapiro, Ansys, Central, Israel

AUTOMATED CLOCK ANALYSIS, SKEW GROUP GENERATION & CT VERIFICATION

Raghubeer Singh, STMicroelectronics, Mumbai, India; Harshil Niranjambhai Upadhyay, STMicroelectronics, Noida, India; Anil Yadav, STMicroelectronics, Gautam Buddha Nagar, India

AUTOMATIC CHECK GENERATION FOR RESET STATES FROM DESIGN DOCUMENTS

Homayoon Akhiani, NVIDIA, Santa Clara, CA

AUTOMATIC TIMING COMPARISON AND VALIDATION TOOL – QUALIFICATION COCKPIT

Adil Bhanji, IBM, Wappinger Falls, NY; Nathan Buck, IBM, Poughkeepsie, NY; Christine Casey, IBM, Raleigh, NC; Eric Foreman, IBM, Fairfax, VA; Anika Hamby, IBM, Burlington, VT; Steven Meyers, IBM, White Plains, NY; Peter Twombly, IBM, Shelburne, VT; Steven Washburn, IBM, Poughquag, NY

AUTOMATION FRAMEWORK BASED IP/SUBSYSTEM INTEGRATION VERIFICATION IN SOC – A SYSTEMATIC APPROACH FOR INTEGRATION QUALITY SIGNOFF

Yogeshwaran Shanmugam, Texas Instruments, Bangalore, India; Aswin B, Texas Instruments, Austin, TX

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

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Keynotes and Visionary Talks

Engineering Track

MONDAY ENGINEERING TRACK POSTER RECEPTION (CONTINUED)

BEST PRACTICES FOR STATIC SIGNOFF

Itai Resh, Hailo, Tel Aviv, Israel

CAPTURING STATISTICAL CHARACTERISTICS OF HIGH-SIGMA RELIABILITY ANALYSIS METHODS

Jeongwoo Heo, Samsung Electronics, Hwaseong, South Korea

COMBINED FEOL/BEOL PROCESS SWEET SPOT SEARCH FOR CHIP PERFORMANCE OPTIMIZATION

Moonsu Kim, Jaeyoung Lim, Jaehyeon Kang, Changho Han, Asheesh Baghel, Synopsys, Wenwen Chai, Synopsys, West Lafayette, IN; Li Ding, Synopsys, Sane Jose, CA

CORRECT BY CONSTRUCTION LAYOUT DESIGN BY AUTO DEVICE PLACEMENT

Urvashi Jindal, NXP Semiconductors, Noida, India; Leonardo Konrad, NXP Semiconductors, Toulouse, France

COMPREHENSIVE, AND AUTOMATED IP AND SOC CONNECTIVITY VERIFICATION SIGN OFF USING FORMAL DV TECHNIQUE

Abhinav Parashar, Parthasarathy Ramesh, Prasanth Kumar Narava, Texas Instruments, Harish Maruthiyodan, Bangalore, India; Ayush Jodh, Texas Instruments, Nagpur, India

CREDIT BASED SCHEDULING FOR PRECISION TIME PROTOCOL FRAMES IN AUTOMOTIVE ETHERNET

Vedansh Seth, Cadence Design Systems, Inc., Varanasi, India; Shubham Agarwal, Cadence Design Systems, Inc., San Jose, CA

DEEP LEARNING PLATFORM FOR FSM-BASED HLS

Khaled Salah, Siemens EDA, San Francisco, CA

DESIGN VERIFICATION WAVEFORM ANALYSIS THROUGH MACHINE LEARNING SOLUTION

Saksham Sangwan, Venkat Padmanabhan, Guha Lakshmanan, Lakshmanan Balasubramanian, Texas Instruments (India) Pvt. Ltd., Bangalore, India

DESIGNING HIGH PERFORMANCE IC PACKAGES ENSURING RELIABILITY AND COST

Manuel Rei, Rachid Taibi, Dassault Systèmes, Paris, France

DESIGNING OPTIMAL SOC ARCHITECTURES FOR COMPUTE-INTENSIVE AI WORKLOADS

Piyush Singh, Sondrel, London, United Kingdom; Rowan Naylor, AI Chip Center for Emerging Smart Systems, Pak Shek Kok, Hong Kong

DLA CIRCUIT OPTIMIZATION FOR AREA AND POWER REDUCTION THROUGH DOUBLE-HEIGHT METAL-LESSER ADDER CELLS

Jaewoo Seo, Samsung Electronics, Hwaseong, South Korea

FAST AND RELIABLE IO RING CHECKER FOR ENSURING ESD ROBUSTNESS AND POWER INTEGRITY COMPLIANCE OF SOC DESIGN

Dhananjay Dubey, Nitin Bansal, Avinash Gupta, Praveen Jakki, Anurag Mittal, Synopsys, Noida, India

FLOORPLAN FOR IMPLEMENTATION METHODOLOGY TO THE NEXT MSOT SMART POWER (BCD) DESIGNS

Livio Fratantonio, STMicroelectronics, Sedriano, Italy; Massimiliano Innocenti, STMicroelectronics, Vercelli, Italy; Riccardo Guglielmo, STMicroelectronics, Milano, Italy; Stefano Basile, Jonhatan Olave, Cadence Design Systems, Inc., Milan, Italy

HIGH PERFORMANCE, SCALABLE AND COST OPTIMIZED AWS CLOUD INFRASTRUCTURE FOR CHIP DEVELOPMENT

Jitendra Mohan, Vivek Trivedi, Vikash Tyagi, Vilesh Shah, Shantanu Divekar, Srimai Inapurapu, Astera Labs, Tanay Sharma, Astera Labs, Santa Clara, CA; Evan Chen, Synopsys, Sunnyvale, CA; Zhiming Shen, Exotanium, Ithaca, NY

LEARNING BOX MODEL USING DSO.AI

Jaemin Seo, Kunhyuk Kang, Hyundon Kim, Jaeseung Choi, Samsung Electronics, Hwaseong, South Korea; Edward Pyo, SB Park, Myoungjun Kwak, Jimmy Kim, Synopsys, Seoul, South Korea; Michael Martin, Synopsys, San Jose, CA; Amzie Adams, Synopsys, Raleigh, NC

MULTI-POLICY LINT SIGNOFF FOR SOCS

Martin Maue, Dream Chip Technologies GmbH, Bremen, Germany; Vikas Sachdeva, Real Intent Inc, Bangalore, India; Yurii Hrytsai, Real Intent Inc, Sunnyvale, CA

NOVEL APPROACH TO IMPROVE THE PROCESS OF REGISTER VERIFICATION IN UVM

Sougata Bhattacharjee, Samsung Semiconductor, Bangalore, India

OPTIMAL MSCTS DRIVER DUPLICATION FOR IMPROVED H-TREE CLOCK SKEW AND INSERTION DELAY

Rohit Murarka, Intel, Karnataka, India; Narendra Nimmagadda, Intel, Fishers, IN; Sai Krishna Kairamkonda, Intel, Hyderabad, India; Raghavendra Vasappanavara, Intel, Santa Clara, CA

PARADIGM SHIFT IN POWER AWARE SIMULATION USING FORMAL TECHNIQUES

Sachin Bansal, Gaurav Pratap, Amit Goldie, Synopsys, Noida, India; Nupur Gupta, Synopsys, Delhi, India; Chirag Patel, Synopsys, Bangalore, India; Vishal Keswani, Synopsys, South Delhi, India

PATH TRACER FOR TR.-LEVEL STA SETUP USING SYNOPSYS NANOTIME

Taehwan Kim, Samsung Electronics, Hwaseong, South Korea

PERFORMANCE AND POWER OPTIMIZING METHOD BY CONTROLLING NANO-SHEET USAGE

Hongseok Choi, Minkook Kim, Sangdo Park, Hyungock Kim, Sangyun Kim, Samsung Electronics, Hwaseong, South Korea

POWER INTEGRITY ANALYSIS OF 3D STACKING STRUCTURE IN CMOS IMAGE SENSOR CHIP

Eric Chen, Omnivision, Shanghai, China; Xiaodong Wang, Ansys, Li Yahui, Ansys, Shanghai, China

Research Sessions

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MONDAY ENGINEERING TRACK POSTER RECEPTION (CONTINUED)

QUALITY ASSURANCE OF DRC DECK BY QA CELL METHODOLOGY AND AUTOMATION USING CADENCE SKILL

Ambika Bhardwaj, Atul Bhargava, STMicroelectronics, Greater Noida, India; Chirag Agarwal, STMicroelectronics, Kerala, India

REQUIREMENT TRACING FOR DESIGN FLOW IN COMMUNICATION PROTOCOLS IP

Marco Meuli, STMicroelectronics, Rome, Italy

RISC-V PROCESSOR CUSTOMIZATION: HOW TO ENABLE HETEROGENEOUS COMPUTE

Zdeněk Příklad, Codasip, Brno, Czech Republic

STATISTICAL OCV BASED DESIGN CLOSURE

Ajoy Mandal, Texas Instruments, Bangalore, India; Nitin Bisht, Texas Instruments, South Delhi, India; Ashwini Kulkarni, Vishwa Prabhat; Mehar Gupta, Cadence Design Systems, Inc., Bangalore, India; Preeti Gupta, Rajat Kukreja, Cadence Design Systems, Inc., Noida, India

THE BENEFITS OF FORMAL SIGNOFF ON NEW AND MATURE DESIGNS

Ping Yeung, NVIDIA, San Francisco, CA; Yvonne Zhang, NVIDIA, Los Angeles, CA; Mark Zhang, NVIDIA, Charlottesville, VA; Hargovind Singh, NVIDIA, Delhi, India; Dharendra Soni, NVIDIA, Gurgaon, India; Vidit Tripathi, NVIDIA, Kanpur Nagar, India; Abhinavnath KT, NVIDIA, Santa Clara, CA; Ujjwal Mittal, NVIDIA, Delhi, India; Arjun Kumar, NVIDIA, Ahmedabad, India

ULTRA-LOW VOLTAGE ENABLEMENT FOR STANDARD CELLS WITH MOMENT BASED LVF

Rohit Kumar Gupta, Chiranjeev Kumar Grover, STMicroelectronics, Noida, India; Etienne Mauir Jean-Arnaud Francois, Olivier Minez, STMicroelectronics, Crolles, France; Sebastien Marchal, STMicroelectronics, Grenoble, France

UNIFIED DESIGN VERIFICATION FLOW FOR PRE-SILICON SOC POWER ESTIMATION AND ACHIEVING POST-SILICON CORRELATION TO CUSTOMER SAMPLING

Prashanth Saraf, Sai Ram Jayanthi, Aruna Koityar, Ninad Khire, Ashwini Padoor, Texas Instruments, Bangalore, India; Ankita Mohanty, Texas Instruments, Vellore, India; Tanushri Bhagat, Texas Instruments, Bhopal, India; Sidhartha Kumar, Texas Instruments, Mumbai, India; Karthik Subburaj, Texas Instruments, Herdon, VA

USING MACHINE LEARNING TO OPTIMIZE AND ACCELERATE RANDOM REGRESSION TESTING

Davide Sanalidro, STMicroelectronics, Milano, Italy; Emilio Stante, STMicroelectronics, Torino, Italy; Maurizio Martina, Polytechnic University of Turin, Torino, Italy

VERIFICATION CHALLENGES & SOLUTIONS OF 10BASET1S AUTOMOTIVE ETHERNET PHY

Harshdeep Verma, Cadence Design Systems, Inc., Noida, India

Research
Sessions

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Session

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Workshop;
Hands-on Labs

Transformative
Technologies
Theater

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Visionary Talks

Engineering
Track

TUESDAY KEYNOTE: HEIKE RIEL AND VISIONARY TALK: PRITH BANERJEE

Time: 8:40 AM – 10:00 AM
Event Type: Keynote, Visionary Talk
Room: 3020, 3rd Floor

INTRODUCTION AND AWARDS

DRIVING ENGINEERING SIMULATION AND DESIGN WITH AI/ML

Prith Banerjee, Ansys, Palo Alto, CA

QUANTUM COMPUTING ROADMAP

Heike Riel, IBM, Zurich, Switzerland

SHOULD BE: A VIEW FROM WALL STREET: THE STATE OF EDA

Time: 10:15 AM – 11:15 AM
Event Type: Analyst Presentation
Topic Area(s): EDA
Room: DAC Pavilion, Level 2 Exhibit Hall

We will examine the financial performance and key business metrics of the EDA industry through 2022, as well as the material technical and market trends and requirements that have influenced EDA business performance and strategies. Among the trends, we will again examine the progression of semiconductor R&D spending and how the market value of the publicly-held EDA companies has evolved. Lastly, we will provide our updated financial projections for the EDA industry for 2023 through 2025. This panel will explore, with four leading software companies, a phenomenon that has long been anticipated: the business, market and technical convergences of the two halves of Engineering Software (EDA and “industrial” software). These convergences are increasingly evident in the companies’ product and acquisition strategies.

Presenter: Jay Vleeschouwer, Griffin Securities, New York, NY

BUILD A CADENCE BURST-TO-CLOUD WORKFLOW WITH NETAPP “DESIGN ANYWHERE” ON AWS

Time: 10:15 AM – 1:15 PM
Event Type: Hands-On Training Session
Topic Area(s): Cloud
Room: 2nd Floor Foyer

Join NetApp, AWS and Cadence to learn how easy hybrid cloud bursting for demanding EDA workloads can be. You will get hands-on experience with setting up and enabling a Cadence Xcellium workflow in a hybrid cloud solution configuration suitable for your most demanding EDA workflows.

Presenter: Jim Holl, NetApp, Los Gatos, CA; Sunghwan Son, AWS; Kushal Koolwal, Cadence

PACKAGING AND MANUFACTURING TECHNOLOGIES SAVE THE DAY!

Time: 10:30 AM – 12:00 PM
Event Type: Engineering Tracks
Topic Area(s): Back-End Design
Room: 2008, Level 2

Organizer(s): Sabya Das, Synopsys, San Francisco, CA

As Semiconductor Technology has been steadily breaking the barrier of a decreasingly lower single digit in the nanometer scale, Manufacturing and Packaging issues are often becoming the determining factor. This session touches upon various aspects of that domain. The first talk discusses the thermal modeling/simulation challenges and opportunities in the context of heterogeneously integrated 3D ICs. The second talk describes advancements in packaging design software, co-design, and analysis methodologies for chips and packages. The objective of the final talk is to facilitate higher productivity and quality in manufacturing. For that, the speaker will discuss the necessary interactions between tape out, manufacturing, and yield analysis phases of the entire solution.

Moderator: Badhri Uppiliappan, BAE Systems, Boston, MA

Panelists: Norman Chang, Ansys, San Jose, CA; Neeraj Kaul, Cadence Design Systems, Inc., Fremont, CA; Andres Torres, Siemens EDA, Wilsonville, OR

DESIGNING EFFECTIVE AUTONOMOUS SYSTEMS AND DIGITAL TWINS

Time: 10:30 AM – 12:00 PM
Event Type: Engineering Tracks
Topic Area(s): Embedded Systems and Software
Room: 2012, 2nd Floor

Organizer(s): Shankar Hemmady, Blue Horizons, San Francisco, CA

This panel will explore the critical role of hardware and system design in the creation and implementation of autonomous systems, and how digital twins can improve the systems development before deployment. Our panelists will discuss the importance of designing hardware systems that are specifically tailored to support such complex systems whose components include sensors, controllers, and other devices that are capable of accurately capturing and communicating data. Panelists will also examine the impact of system design on the accuracy and reliability of such systems: how a good design can enable real-time data collection and analysis, as well as support integration with other essential subsystems and technologies like AI-ML and IoT.

Finally, panelists will discuss the challenges and opportunities for innovation in design techniques and methodologies as such systems continues to evolve and grow in importance.

Moderator: Nitin Dahad, EE Times, London, United Kingdom

Panelists: Anna-Katrina Shedletsky, Instrumental Inc., Mountain View, CA; Amit Goel, NVIDIA, Santa Clara, CA; David Fritz, Siemens EDA, San Diego, CA; Prith Banerjee, Ansys, Palo Alto, CA; Yogesh Goel, Cadence Design Systems, Inc., Fremont, CA

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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DESIGN FOR VERIFICATION – CASE REOPENED

Time: 10:30 AM – 12:00 PM

Event Type: Engineering Tracks

Topic Area(s): Front-End Design

Room: 2010, 2nd Floor

Organizer(s): Nicola Nicolici, McMaster University, Hamilton, Canada

There is a need to evolve the verification methodologies of complex system-on-a-chip (SoC) devices and add new dimensions to the mindsets employed across different stages of verification. A major complexity is now added to the SoC design and SoC verification challenges by industry's adopting chiplet-based SoC design. Design for Verification (DfV) is a natural evolution in both design and verification methodologies. The central idea of DfV is that specialized hardware blocks can be leveraged across different stages of design verification (IP block, SoC, emulation, silicon prototype) not only to address the transfer of verification test plans/data between different environments (e.g., pre-silicon vs emulation vs post-silicon) but also to make the verification more effective and efficient at each of these verification stages. While different aspects of DfV have been employed across multiple projects in different organizations (possibly even unknowingly on some occasions), it is important to bring different stakeholders together to share thoughts and improve the collective understanding of DfV and articulate its long-term benefits.

Moderator: Nicola Nicolici, McMaster University, Hamilton, Canada

Panelists: Sankaran Menon, Intel, Austin, TX; Amit Sharma, Synopsys, Mountain View, CA; Pouya Taatizadeh, Google, Mountain View, CA; David Akselrod, AMD, Toronto, Canada

ADVENTURES IN HETEROGENEOUS COMPUTING SYSTEMS

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): SoC, Heterogeneous, and Reconfigurable Architectures

Room: 3006, 3rd Floor

Session Chair(s): Francesco Restuccia, University of California, San Diego; Jeronimo Castrillon, Technische Universität Dresden

Heterogeneous MPSoCs offer the advantages of high-performance and energy-efficiency compared to homogeneous MPSoCs that consist of a single CPU core type. However, programming and architecting heterogeneous MPSoCs are challenging topics in their own right. The papers in this session explore application mapping, hardware acceleration, memory bandwidth modulation, an last-level cache (LLC) integration for heterogeneous systems. These innovations provide numerous insights on how to optimize the performance of heterogeneous MPSoCs as technology and workload complexity evolves.

LIGHTNING TALK – THE NEED FOR AND CHALLENGES OF HETEROGENEOUS SYSTEMS

Derek Chiou, The University of Texas at Austin, TX

MAP-AND-CONQUER: ENERGY-EFFICIENT MAPPING OF DYNAMIC NEURAL NETS ONTO HETEROGENEOUS MPSOCS

Halima Bouzidi, Université Polytechnique Hauts-de-France, Valenciennes, France; **Mohamad Odema**, Mohammad Al Faruque, University of California, Irvine, CA; **Hamza Ouarnoughi**, INSA Hauts-de-France, Valenciennes, France; **Smail Niar**, INSA Hauts-de-France, CNRS, Valenciennes

SPECIALIZATION MEETS FLEXIBILITY: A HETEROGENEOUS ARCHITECTURE FOR HIGH-EFFICIENCY, HIGH-FLEXIBILITY AR/VR PROCESSING

Arpan Suravi Prasad, ETH Zürich, Switzerland; **Luca Benini**, University of Bologna, ETH Zürich, Bologna, Italy; **Francesco Conti**, University of Bologna, Italy

FINE-GRAINED QOS CONTROL VIA TIGHTLY-COUPLED BANDWIDTH MONITORING AND REGULATION FOR FPGA-BASED HETEROGENEOUS SOCS

Gianluca Brilli, Alessandro Capotondi, Paolo Burgio, Paolo Valente, Andrea Marongiu, University of Modena and Reggio Emilia, Modena, Italy; **Giacomo Valente**; **Tania Di Mascio**, University of L'Aquila, Italy

ARCHITECTING SELECTIVE REFRESH BASED MULTI-RETENTION CACHE FOR HETEROGENEOUS SYSTEM

Sukarn Agarwal, University of Edinburgh, United Kingdom; **Shounak Chakraborty**, Magnus Själander, Norwegian University of Science and Technology, Trondheim, Norway

Research Sessions

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Engineering Track

BREAKING NEWS FROM RTL TECHNOLOGY-INDEPENDENT OPTIMIZATION

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): RTL/Logic Level and High-level Synthesis

Room: 3002, 3rd Floor

Session Chair(s): Giovanni de Micheli, École Polytechnique Fédérale de Lausanne; Cunxi Yu, University of Utah

New exciting progress in GPU-parallel algorithms for And-Inverter Graphs (AIGs) technology-independent logic optimization, database-dependent AIG-based window rewriting, AIG-based minimization of factored form literal count, and DC-aware extraction of EXOR-SOPs (ESOPs).

LIGHTNING TALK – EQUALITY SATURATION FOR DATAPATH SYNTHESIS: A PATHWAY TO PARETO OPTIMALITY

Zhiru Zhang, Cornell University, Ithaca, NY

*RETHINKING AIG RESYNTHESIS

Tianji Liu, Young, The Chinese University of Hong Kong; **Evangeline Young**, The Chinese University of Hong Kong

A DATABASE DEPENDENT FRAMEWORK FOR K-INPUT MAXIMUM FANOUT-FREE WINDOW REWRITING

Xuliang Zhu, Ruofei Tang, Xin Huang, Jianliang Xu, Hong Kong Baptist University, Hong Kong; **Lei Chen**, Xing Li, Mingxuan Yuan, Weihua Sheng, Huawei, Hong Kong

IMPROVING STANDARD-CELL DESIGN FLOW USING FACTORED FORM OPTIMIZATION

Alessandro Tempia Calvino, Giovanni De Micheli, École Polytechnique Fédérale de Lausanne, Switzerland; **Alan Mishchenko**, University of California, Berkeley, CA; **Herman Schmit**, **Ethan Mahintorabi**, **Xiaoqing Lu**, Google, Mountain View, CA

DON'T-CARE AWARE ESOP EXTRACTION VIA REDUCED DECOMPOSITION-TREE EXPLORATION

Chun-Yu Wei, Jie-Hong Roland Jiang, National Taiwan University, Taipei, Taiwan

CIRCUIT DESIGN POTPOURRI

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML, Digital, and Analog Circuits

Room: 3010, 3rd Floor

Session Chair(s): Suriyaprakash Natarajan, Intel; Marcus Pan, Semiconductor Research Corporation

This session presents a potpourri of solutions to improve performance, power, and area for digital/analog circuits and packaging. The research spans a broad range of topics, including reducing power for deep neural network hardware accelerators, glass interposers for 3D stacking of chiplets, and analog circuit parameter optimization method with reinforcement learning.

LIGHTNING TALK – SYSTEM-LEVEL INNOVATION FOR THE NEXT DECADE AI PERFORMANCE, POWER, AREA WITH CO-OPTIMIZATION

Marcus Pan, Semiconductor Research Corporation, Durham, NC

POWERPRUNING: SELECTING WEIGHTS AND ACTIVATIONS FOR POWER-EFFICIENT NEURAL NETWORK ACCELERATION

Richard Petri, Ulf Schlichtmann, Bing Li, Technische Universität München, Germany; **Grace Li Zhang**, Technische Universität Darmstadt, Darmstadt, Germany; **Yiran Chen**, Duke University, Durham, NC

CPE: AN ENERGY-EFFICIENT EDGE-DEVICE TRAINING WITH MULTI-DIMENSIONAL COMPRESSION MECHANISM

Zhou Wang, Jingchuan Wei, Leibo Liu, Shaojun Wei, Shouyi Yin, Tsinghua University, Beijing, China; **Boxiao Han**, Hongjun He, China Mobile Research Institute, Beijing, China

GLASS INTERPOSER INTEGRATION OF LOGIC AND MEMORY CHIPLTS: PPA AND SIGNAL/POWER INTEGRITY BENEFITS

Pruek Vanna-iampikul, Lingjun Zhu, Serhat Erdogan; Mohanalingam Kathaperumal, Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA; **Ravi Agarwal**, Ram Gupta, Meta, Menlo Park, CA; **Kevin Rinebold**, Siemens EDA, Southport, NC

ROSE: ROBUST ANALOG CIRCUIT PARAMETER OPTIMIZATION WITH SAMPLING-EFFICIENT REINFORCEMENT LEARNING

Jian Gao, Weidong Cao, Xuan Zhang, Washington University, St. Louis, MO

* Denotes a Best Paper Candidate

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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LEARNING WITH DRIVES AND CONVERTIBLES – FROM NEAR DATA TO CLOUD

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): Embedded Memory, Storage and Networking
Room: 3008, 3rd Floor

Session Chair(s): Zili Shao, The Chinese University of Hong Kong; Chien-Chung Ho, National Chung Cheng University

Can learning based approaches help in improving solid state drive performance? The first three papers employ reinforcement learning to perform several critical solid state drive tasks - lifetime prediction on SSD devices, conversion of flash memory cells in convertible SSDs, and fairness control. The fourth paper explores reducing data transfer overheads through local processing in computational SSDs.

LIGHTNING TALK – MODEL, FRAMEWORK AND INTEGRATION FOR IN-STORAGE COMPUTING WITH COMPUTATIONAL SSDS

Zili Shao, City University of Hong Kong, Hong Kong

LEARNING-BASED DATA SEPARATION FOR WRITE AMPLIFICATION REDUCTION IN SOLID STATE DRIVES

Penghao Sun, Litong You, Shengan Zheng, Wanru Zhang, Ruoyan Ma, Linpeng Huang, Shanghai Jiao Tong University, Shanghai, China; Jie Yang, Guanzhong Wang, Feng Zhu, Shu Li Alibaba Group, Shanghai, China

REINFORCEMENT LEARNING-ASSISTED MANAGEMENT FOR CONVERTIBLE SSDS

Qian Wei, Zhiping Jia, Mengying Zhao, Zhaoyan Shen, Shandong University, Qingdao, China; Yi Li, Bingzhe Li, Oklahoma State University, Stillwater, OK

FAIR WILL GO ON: A COLLABORATION-AWARE FAIRNESS SCHEME FOR NVME SSD IN CLOUD STORAGE SYSTEM

Yang Zhou, Fang Wang, Zhan Shi, Dan Feng, Huazhong University of Science and Technology, Wuhan, China; Yu Du, Alibaba Group, Shanghai, China

OPTIMIZING THE PERFORMANCE OF NDP OPERATIONS BY RETRIEVING FILE SEMANTICS IN STORAGE

Lin Li, Xianzhang Chen, Jiali Li, Jiapin Wang, Duo Liu, Yujian Tan, Ao Ren, Chongqing University, Chongqing, China

NEW DISCOVERIES IN CLASSICAL HARDWARE SECURITY PROBLEMS

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): Hardware Security: Primitives, Architecture, Design & Test

Room: 3012, 3rd Floor

Session Chair(s): Ning Zhang, Washington University St. Louis; Reza Azarderakhsh, Florida Atlantic University

Classical problems last with new meanings and applications. This session has four papers on three classical hardware security problems: IP protection, side-channel analysis, and hardware true random number generator. The first paper reports a new obfuscation mechanism to establish trust with low overhead. ActiWate presented in the second paper is a new watermark-based SoC IP protection that can be verified by system peripherals. Authors in the third paper discover a new problem in SPICE simulation for side-channel analysis. The last paper shows a novel architecture to generate true random numbers by ring oscillators with high throughput and energy efficiency.

LIGHTNING TALK – THE INCREDIBLE SHRINKING BLACK BOX MODEL

Patrick Schaumont, Worcester Polytechnic Institute, Worcester, MA

HYBRID OBFUSCATION OF CHIPLET-BASED SYSTEMS

Yousef Safari, Boris Vaisband, McGill University, Montreal, Canada; **Pooya Aghanoury**, Subramanian Iyer, Nader Sehatbakhsh, University of California, Los Angeles, CA

ACTIWATE: ADAPTIVE AND DESIGN-AGNOSTIC ACTIVE WATERMARKING FOR IP OWNERSHIP IN MODERN SOCS

Zahin Ibnat, Mohammad Rahman, Mridha Md Mashahedur Rahman, Hadi Mardani Kamali, Mark Tehranipoor, Farimah Farimandi, University of Florida, Gainesville, FL

ON THE UNPREDICTABILITY OF SPICE SIMULATIONS FOR SIDE-CHANNEL LEAKAGE VERIFICATION OF MASKED CRYPTOGRAPHIC CIRCUITS

Kazuki Monta, Makoto Nagata, Kobe University, Kobe, Japan; Josep Balasch, Ingrid Verbauwhede, KU Leuven, Belgium

AN ULTRA HIGH-THROUGHPUT AND ENERGY-EFFICIENT TRNG EXPLOITING FOUR FPGA-COMPATIBLE RING OSCILLATORS AND ONE MULTIPHASE SAMPLER

Zhaojun Lu, Houjia Qidiao, Qidong Chen, Zhenglin Liu, Jiliang Zhang, Huazhong University of Science and Technology, Wuhan, China

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THE CROSSROAD OF AI PARADIGMS: FROM NEURONS TO BITS

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Algorithms

Room: 3004, 3rd Floor

Session Chair(s): Saurav Nanda, Synopsys; Grace Li Zhang, Technische Universität Darmstadt

As hardware performance slows in the post-Moore era, we need to explore new computing paradigms in order to further improve the energy efficiency of artificial intelligence. In this session, novel brain-inspired and physics-based computing paradigms are well discussed from an algorithmic perspective. The presentations in this session focus on the optimization and acceleration of spiking neural networks (the first paper), hyperdimensional computing (the second and the third papers), and ising machine learning (the fourth paper).

LIGHTNING TALK – BRIDGING NEURO-DYNAMICS AND COGNITION

Mohsen Imani, University of California, Irvine, CA

NEUROGENESIS DYNAMICS-INSPIRED SPIKING NEURAL NETWORK TRAINING ACCELERATION

Shaoyi Huang, Kaleel Mahmood, Bin Lei, Caiwen Ding, University of Connecticut, Storrs, CT; Haowen Fang, Synopsys, Sunnyvale, CA; Bowen Lei, Texas A&M University, College Station, TX; Nuo Xu, Yue Sun, Wujie Wen, Lehigh University, Bethlehem, PA; Dongkuan Xu, North Carolina State University, Raleigh, NC

AN EXTENSION TO BASIS-HYPERVECTORS FOR LEARNING FROM CIRCULAR DATA IN HYPERDIMENSIONAL COMPUTING

Igor Nunes, Mike Heddes, Tony Givargis, Alexandru Nicolau, University of California, Irvine, CA

DISTHD: A LEARNER-AWARE ENCODING METHOD FOR HYPERDIMENSIONAL CLASSIFICATION

Junyao Wang, Sitao Huang, Mohsen Imani, University of California, Irvine, CA

ISING-CF: A PATHBREAKING COLLABORATIVE FILTERING METHOD THROUGH EFFICIENT ISING MACHINE LEARNING

Zhuo Liu, Zhenyu Pan, Anshujit Sharma, Michael Huang, **Tong Geng**, University of Rochester, NY; Yunan Yang, ETH Zürich, Switzerland; Amit Hasan, Caiwen Ding, University of Connecticut, Storrs, CT; Ang Li, Pacific Northwest National Laboratory, Richland, WA

THE QUANTUM COMPILATION REVOLUTION: TRANSFORMING COMPUTING AS WE KNOW IT

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): Quantum Computing

Room: 3003, 3rd Floor

Session Chair(s): to be announced

This session explores cutting-edge developments in quantum compilation, showcasing new techniques for optimizing quantum computation. Topics covered range from compression-aided frameworks to combat fluctuating quantum noise to layout synthesis techniques for near-term quantum processors.

LIGHTNING TALK – SCALING UP QUANTUM COMPILATION – CHALLENGES AND OPPORTUNITIES

Jason Cong, The University of California, Los Angeles, CA

BATTLE AGAINST FLUCTUATING QUANTUM NOISE: COMPRESSION-AIDED FRAMEWORK TO ENABLE ROBUST QUANTUM NEURAL NETWORK

Zhirui Hu, Weiwen Jiang, George Mason University, Fairfax, VA; Lin Youzuo, Los Alamos National Laboratory, Los Alamos, NM; Qiang Guan, Kent State University, Kent, OH

COMPILER OPTIMIZATION FOR QUANTUM COMPUTING USING REINFORCEMENT LEARNING

Nils Quetschlich, Robert Wille, Technische Universität München, Munich, Germany; Lukas Burgholzer, Johannes Kepler University Linz, Linz, Austria

ORCHESTRATING MEASUREMENT-BASED QUANTUM COMPUTATION OVER PHOTONIC QUANTUM PROCESSORS

Yingheng Li, Aditya Pawar, Mohadeseh Azari, Yanan Guo, Youtao Zhang, Jun Yang, Kaushik Seshadreesan, Xulong Tang, University of Pittsburgh, PA

SCALABLE OPTIMAL LAYOUT SYNTHESIS FOR NISQ QUANTUM PROCESSORS

Wan-Hsuan Lin, Jason Kimko, Bochen Tan, Jason Cong, University of California, Los Angeles, CA; Nikolaj Bjorner, Microsoft, Redmond, WA

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

DAC60 CELEBRATION PANEL: DESIGNING THE FUTURE

Time: 10:30 AM – 12:00 PM

Event Type: Research Panel

Topic Area(s): EDA

Room: 3014, 3rd Floor

Organizer/Moderator: Subhasish Mitra, Stanford University, Stanford, CA

EDA, in tandem with silicon integrated circuits, has made possible computers, the Internet, smartphones, cloud computing, and deep learning (now broadly termed AI).

So, what's next?

Panelists: Alberto Sangiovanni-Vincentelli, University of California, Berkeley, CA; E.J. Chichilnisky, Stanford University, Stanford, CA; Arvind Mithal, Massachusetts Institute of Technology, Cambridge, MA; Jan Rabaey, imec; University of California, Berkeley, CA; Ingrid Verbauwhede, KU Leuven, Belgium; Douglas C.H. Yu, TSMC, Hsinchu, Taiwan

TOWARD PROVABLY CORRECT HARDWARE ACCELERATOR DESIGN: PERSPECTIVES, OPPORTUNITIES, AND CHALLENGES

Time: 10:30 AM – 12:00 PM

Event Type: Special Session (Research)

Topic Area(s): EDA

Room: 3001, 3rd Floor

We are in a golden era of rapid accelerator architecture innovations driven by emerging applications where the pure pursuit of FLOPS in hardware design with generality and abstraction is being replaced with targeted specialization both in academia and in industry. Hardware accelerators have become one of the most critical functional blocks of modern heterogeneous computer architectures. These accelerators implement domain-specific functions for machine learning and inference, edge intelligence, secure computing, and so on to improve power efficiency and computation throughput by several orders of magnitude. At the same time, the existing design practice cannot keep up with the proliferation of accelerators and the pace of accelerator innovations due to the exponentially increasing complexity and cost. In particular, verification of functional correctness of accelerators has become a major factor in design complexity and cost, and the trend is worsening.

This calls for a design paradigm shift, including raising the abstraction level of hardware accelerator design to software and a new programming model amenable to scalable and composable rapid verification. Such requirements were summarized in a 2018 DARPA article, "... priorities we set today will determine whether the state of the electronics ecosystem becomes stagnant, rigid, and traditional, or grows to be dynamic, flexible, and innovative."

Recent work published in multiple premier venues such as DAC, DATE, ICCD, ICCAD, FMCAD, ISCA, MICRO, PLDI, and many more from domain-specific languages and compilers, architecture, and formal methods communities, indicate a growing number of researchers with common interests at the intersection of accelerator architecture, design, and verification. We intend this special session to provide a forum to bring researchers from these communities together to cross-pollinate ideas. We believe that only with the interdisciplinary collaboration we can arrest the design complexity and cost trend to keep up with the pace of accelerator architectural innovations.

Organizer(s): Debjit Pal, University of Illinois at Chicago; Wen Wang, Intel

GENERALIZING THE ISA TO THE ILA: A SOFTWARE/HARDWARE INTERFACE FOR ACCELERATOR-RICH PLATFORMS

Sharad Malik, Princeton University, Princeton, NJ

VERIFICATION OF AEROSPACE SAFETY CRITICAL SYSTEMS: CHALLENGES AND OPPORTUNITIES FOR ACCELERATORS

Keith Rebello, The Boeing Company, Washington, DC

A SCALABLE FORMAL APPROACH FOR CORRECTNESS-ASSURED HARDWARE DESIGN

Jin Yang, Intel, Hillsboro, AL

Research Sessions

Special Session

Panel

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Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

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Keynotes and Visionary Talks

Engineering Track

REVOLUTIONIZING EDA: THE POWER OF AI, ML, AND NLP

Time: 10:30 AM – 11:15 AM

Event Type: Transformative Technologies Theater

Topic Area(s): EDA

Room: Transformative Technologies Theater, Level 1 Exhibit Hall

The integration of AI, ML, and NLP techniques in EDA has the potential to significantly improve the efficiency, innovation, and quality of electronic systems. Customers in the semiconductor and EDA industries can benefit from reduced design time, increased reliability, and enhanced performance. This talk will draw upon use cases and research that have shown the integration of AI, ML, and NLP techniques in EDA has led to significant improvements in design accuracy. For example, ML algorithms have been used to optimize routing in complex circuits, while NLP techniques have been used to extract relevant design information from textual specifications. The talk will cover the use of unsupervised, supervised, and reinforcement learning techniques and NLP techniques in EDA tools and workflows.

Presenter: Majid Ahadi Dolatsara, Keysight Technologies, Los Angeles, CA

DIY ORBITAL TRACKING SYSTEM FOR SPACE COMMUNICATION: A PROJECT TO CONTACT THE INTERNATIONAL SPACE STATION

Time: 11:30 AM – 12:30 PM

Event Type: TechTalk

Room: DAC Pavilion, Level 2 Exhibit Hall

Zeke Wheeler was 8 years-old when he asked his dad how he could call the astronauts on the International Space Station (ISS). This casual question resulted in a three-year epic STEM-learning adventure to contact the ISS, which included obtaining an FCC license to operate a radio, creating a satellite tracker using Legos, and researching, designing and building original circuit boards and antennas with his dad using Cadence Microwave Office. There have been trials as well as triumphs in this ongoing project of fortitude and resilience.

Presenter: Zeke Wheeler

ENTERING A NEW ERA WITH EDA 2.0 AND AI-DRIVEN ELECTRONIC SYSTEM DESIGN

Time: 1:00 PM – 1:45 PM

Event Type: SKYTalk

Topic Area(s): AI, EDA

Room: DAC Pavilion, Level 2 Exhibit Hall

At Cadence, we see a great opportunity for our industry to enter a new era of EDA 2.0, defined by AI-driven platforms that optimize horizontally across multiple runs of many tools throughout an entire system design program. Learn how EDA 2.0 is bringing all design and verification data together under a unified data platform—RTL, layouts, constraints, waveforms, coverage, reports, log files, state graphs, AI models, and metadata with our new Cadence Joint Enterprise Data and AI (JedAI) Platform.

Presenter: Paul Cunningham, System Verification Group, Mountain View, CA

ARE WE THERE YET? FROM CLOUD-COMPATIBLE TO CLOUD-OPTIMIZED

Time: 1:00 PM – 1:45 PM

Event Type: Transformative Technologies Theater

Topic Area(s): Cloud

Room: Transformative Technologies Theater, Level 1 Exhibit Hall

Organizer: Leigh Anne Clevenger, Silicon Integration Initiative, Inc., Albany, NY

EDA tools can all run on the cloud. The inherent cloud compatibility is a great start, but a lot needs to be done to make EDA tools cloud native. Simply put, most EDA tools were not built for the cloud. Features such as horizontal scalability are most effective when designed from the start. As more and more design companies start to leverage cloud and the flexible pay-per-use licensing, there is a better understanding of chip design on cloud. Hear from a panel of cloud and EDA companies as they debate the state of the art of EDA on Cloud and the improvements needed.

Moderator: Natesan Venkateswaran, IBM, Hopewell Junction, NY

Panelists: Richard Paw, Microsoft, Cupertino, CA; Dean Hildebrand, Google, Mountain View, CA; Murat Becer, Ansys, Los Altos, CA; Amit Varde, Keysight, San Francisco, CA

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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MICROFAAS SERVER-LESS COMPUTING, RISC-V VIRTUAL PLATFORMS, AND FLEXIBLE SYSTEMS MODELING PLATFORM.

Time: 1:30 PM – 3:00 PM

Event Type: Embedded Systems and Software

Topic Area(s): Embedded Systems and Software

Room: 2008, Level 2

Session Chair(s): ChengYeh Wang (Mediatek)

In this session, we will discuss a wide variety of topics ranging from MicroFaaS – serverless computing, RISC-V Android virtual platforms, OpenAI, ChatGPT, cost-effective Open source AutoSAR standard implementation of new concepts and features and Avionics Systems and system modeling and simulation platforms.

EARLY ANDROID SOFTWARE VERIFICATION WITH RISC-V VIRTUAL PLATFORMS

Lukas Juenger, Jan Henrik Weinstock, MachineWare GmbH, Aachen, Germany

MICROFAAS ON OPENFAAS: AN EMBEDDED PLATFORM FOR CLOUD FUNCTIONS

Abin Binoy, Anthony Byrne, **Ayse Coskun**, Boston University, Boston, MA

USING CHATGPT AND OPENAI TO WRITE EMBEDDED SOFTWARE

Mark Kraeling, GE Transportation, Melbourne, FL

DEFINING AVIONICS SYSTEM ARCHITECTURE FOR MULTIPLE USE CASES WITH STRINGENT REQUIREMENTS USING SYSTEM MODELLING

Deepak Shankar, Mirabilis Design Inc., Chennai, India; Tom Jose, Mirabilis Design Inc., Tamil Nadu, India

AUTOSAR CLASSIC PLATFORM DEMONSTRATOR

Moisés Ignacio Urbina Fuentes, ALTEN Group, Cologne, Germany

ADVANCED VERIFICATION AND DEBUG

Time: 1:30 PM – 3:00 PM

Event Type: Engineering Tracks

Topic Area(s): Front-End Design

Room: 2010, 2nd Floor

Session Chair(s): Puneet Anand (AMD)

Join us to learn about new strategies in the catch-up game verification engineers play daily with the increasing design complexity and tighter schedules. For serious gamers, tackling performance is the key to a game well played.

AN AUTOMATED FLOW FOR HIGH PERFORMANCE ASYNCHRONOUS DIGITAL CONTROLLERS

Enea Dimroci, Roberta Priolo, Francesco Battini, STMicroelectronics, Milano, Italy

NOVEL NUMERICAL HARDWARE DESIGN METHODOLOGY: FROM MACHINE READABLE SPECIFICATION TO OPTIMIZED RTL

Theo Drane, Intel, Folsom, CA

SOPHISTICATE PERFORMANCE VERIFICATION OF SOC BUS BY IP-XACT AND MODEL

Hyungtae Park, Hyunjin Kim, Taehwa Ko, Hyunjae Woo, Youngsik Kim, Seonil Choi, Samsung Electronics, Hwaseong, South Korea

DEBUG ACCELERATOR & PERFORMANCE VALIDATOR

Ratan Deep, Samsung Semiconductor, Bangalore, India; Harsh Setia, Samsung Semiconductor, Bangalore, India; Shashank N, Samsung Semiconductor, Bangalore, India; **Sudhakar Bansal**, Samsung Semiconductor, Bangalore, India

EMULATION BASED AUTOMATION PLATFORM FOR SOC PERFORMANCE VERIFICATION

Jisu Yang, Jeonggu Lee, Seolgyeong Jeong, Hyunjae Woo, Youngsik Kim, Seonil Choi, Samsung Electronics, Hwaseong, South Korea

A JOINT IP XACT/RTL DESIGN FLOW FOR LARGE SOC

Ping Ling, Intel, Bayan Lepas, Malaysia; Mael Rabe, Valentin Boyer, Chouki Aktouf, Defacto Technologies, Grenoble, France

Research Sessions

Special Session

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Engineering Track

IMPLEMENTATION ASPECTS FOR LEADING-EDGE IP

Time: 1:30 PM – 3:00 PM
Event Type: Engineering Tracks
Topic Area(s): IP
Room: 2012, 2nd Floor

Session Chair(s): Navid Farazmand (Intel)

IP vendors provide verified IP. During digital and analog implementation, the rubber hits the road. This session will discuss key implementation aspects, including DFT for memories in automotive, weak link detection in memory periphery, SoC sign-off aspects, layout closure turn-around-time, noise analysis, and automation of the creation of chiplet interfaces across technology nodes.

ADVANCED DFT METHOD USING CHECKER AND INDICATION FFS ON AUTOMOTIVE NAND FLASH MEMORY

Yong Lee, SK hynix, Seongnam-si, South Korea; Joon Kim, Synopsys, Seongnam-si, South Korea; Seokjun Jang, Sungho Kang, Yonsei University, Seoul, South Korea

WEAK LINK DETECTION IN MEMORY PERIPHERY USING DESIGN ROBUSTNESS ANALYSIS

Ashish Kumar, Shashank Gupta, Rohit Kumar Gupta, STMicroelectronics, Noida, India; Rakesh Shenoy, Synopsys, Noida, India; Rayson Yam, Synopsys, San Francisco, CA

THE ART OF BREAKING THINGS DOWN - HIERARCHICAL ABSTRACTION FOR POWER SENSITIVE SOC SIGNOFF

Gaurav Pratap; Sachin Bansal, Amit Goldie, Synopsys, Noida, India; Nupur Gupta, Synopsys, Delhi, India; Chirag Patel, Synopsys, Bangalore, India; Vishal Keswani, Synopsys, South Delhi, India

FAST AND ACCURATE PHASE NOISE ANALYSIS OF CRYSTAL OSCILLATOR IN 28 FDSOI PROCESS

Sahil Kumar; Nitin Jain, Atul Bhargava, STMicroelectronics, Greater Noida, India; Prayes Jain, Cadence Design Systems, Inc., Noida, India

AUTOMATIC CHIPLET INTERFACE IP GENERATION ACROSS TECHNOLOGY NODES, VENDORS, AND STACKS USING INTELLIGENT IP

Benjamin Prautsch, Andy Heinig, Fraunhofer IIS/EAS, Dresden, Germany

ACCELERATORS, ACCELERATORS AND MORE ACCELERATORS!

Time: 1:30 PM – 3:00 PM
Event Type: Research Manuscript
Topic Area(s): SoC, Heterogeneous, and Reconfigurable Architectures
Room: 3012, 3rd Floor

Session Chair(s): Hassan Nassar, Karlsruhe Institute of Technology; Jeferson Gonzalez, Karlsruhe Institute of Technology

This session presents significant advancements in application-specific accelerators and acceleration technologies. With the end of Moore's Law, advances in general-purpose computing are slowing, with application-specific hardware accelerators emerging as an alternative. This session presents accelerations for workloads in bioinformatics, image processing, and operating system thread management, as well as a novel methodology to map polyhedral loops to a programmable Coarse Grained Reconfigurable Array (CGRA) accelerator.

LIGHTNING TALK – THE ACCELERATOR LANDSCAPE – A SYSTEM-LEVEL PERSPECTIVE

Andreas Gerstlauer, The University of Texas at Austin, TX

PROFILE-DRIVEN BANDED SMITH-WATERMAN ACCELERATION FOR SHORT READ ALIGNMENT

Konstantina Koliogeorgi, Dimitrios Soudris, Sotirios Xydis, Harokopio University of Athens, Greece

FAST FPGA ACCELERATOR OF GRAPH CUT ALGORITHM WITH OUT-OF-ORDER PARALLEL EXECUTION IN FOLDING GRID ARCHITECTURE

Guangyao Yan, Xinzhe Liu, Yajun Ha, Shanghai Tech University, Shanghai, China; Hui Wang, Shanghai Advanced Research Institute, Shanghai, China

OPTIMIZING DATA REUSE FOR CGRA MAPPING USING POLYHEDRAL-BASED LOOP TRANSFORMATIONS

Liao Huang, Dajiang Liu, Chongqing University, Chongqing, China

HAWEN: HARDWARE ACCELERATOR FOR THREAD WAKE-UPS IN LINUX EVENT NOTIFICATION

Lars Nolte, Tim Twardzik, Clara Kowalsky, Thomas Wild, Andreas Herkersdorf, Technische Universität München, Germany; Camille Jalier, Huawei, Jiyuan Shi, Grenoble, France; Zhigang Huang, Huawei, Nanjing, China

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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ALL ROUTES TO TIMING CLOSURE

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): Timing and Low Power Design

Room: 3002, 3rd Floor

Session Chair(s): Yibo Lin, Peking University; Krishnan Sundaresan, Ampere Computing

This session presents advanced methods for timing closure, from analysis, prediction, to optimization. The first presentation employs machine learning to co-optimize data and clock to achieve improved results. The next two papers use new machine learning algorithms to predict timing at different design stages, helping timing closure. The last presentation uses transfer and active learning techniques to optimize the timing across corners.

LIGHTNING TALK – ALL ROUTES TO TIMING CLOSURE

Iris Hui-Ru Jiang, National Chiao Tung University, Taipei, Taiwan

*RL-CCD: CONCURRENT CLOCK AND DATA OPTIMIZATION USING ATTENTION-BASED SELF-SUPERVISED REINFORCEMENT LEARNING

Yi-Chen Lu, Georgia Institute of Technology, Atlanta, GA; **Wei-Ting Chan**, Synopsys, Hillsboro, OR; **Deyuan Guo**, Sudoipto Kundu, Synopsys, Mountain View, CA; **Vishal Khandelwal**, Synopsys, Hillsboro, CA; **Sung Kyu Lim**, Georgia Institute of Technology, Atlanta, GA

RESTRUCTURE-TOLERANT TIMING PREDICTION VIA MULTIMODAL FUSION

Ziyi Wang, Siting Liu, Yuan Pu, Tsung-Yi Ho, Bei Yu, The Chinese University of Hong Kong; **Song Chen**, University of Science and Technology of China, Hefei, China

CRITICAL PATHS PREDICTION UNDER MULTIPLE CORNERS BASED ON BILSTM NETWORK

Qianqian Song, Xu Cheng, Peng Cao, Southeast University, Nanjing, China

TOTAL: MULTI-CORNERS TIMING OPTIMIZATION BASED ON TRANSFER AND ACTIVE LEARNING

Wei Xing, Zhelong Wang, Weisheng Zhao, Yuanqing Chen, Beihang University, Beijing, China; **Rongqi Lu**, Sichuan Normal University, Chengdu, China; **Zheng Xing**, Rockchip Electronics Co., Ltd, Fuzhou, China; **Ning Xu**, Wuhan University of Technology, Wuhan, China

AN ODYSSEY IN QUANTUM CIRCUITS: UNLEASHING THE POWER OF QUANTUM COMPUTING

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): Quantum Computing

Room: 3006, 3rd Floor

Session Chair(s): Robert Wille, Technische Universität München

This session covers techniques for optimization of quantum circuits. Presentations range from optimizations to improve simulations of molecular dynamics problems to synthesis algorithms for multi-qubit gates.

LIGHTNING TALK – AN ODYSSEY IN QUANTUM CIRCUITS: UNLEASHING THE POWER OF QUANTUM COMPUTING

Edoardo Chabon, EPFL, Lausanne, Switzerland

EVER MORE OPTIMIZED SIMULATIONS OF FERMIONIC SYSTEMS ON A QUANTUM COMPUTER

Qingfeng Wang, Ze-Pei Cian, Yunseong Nam, University of Maryland, College Park, MD; **Ming Li**, Atom Computing, Berkeley, MD; **Igor Markov**, Nova Ukraine, Mountain View, CA

OPTIMAL SYNTHESIS OF MULTI-CONTROLLED QUDIT GATES

Wei Zi, Qian Li, Xiaoming Sun, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

QUIXOTE: IMPROVING FIDELITY OF QUANTUM PROGRAM BY INDEPENDENT EXECUTION OF CONTROLLED GATES

Enhyeok Jang, Seungwoo Choi, Won Woo Ro, Yonsei University, Seoul, South Korea

HYBRID GATE-PULSE MODEL FOR VARIATIONAL QUANTUM ALGORITHMS

Zhiding Liang, Ruiyang Qin, Yiyu Shi, University of Notre Dame, South Bend, IN; **Zhixin Song**, Georgia Institute of Technology, Atlanta, GA; **Jinglei Cheng**, Yiru Wang, Xuehai Qian, Purdue University, West Lafayette, IN; **Zichang He**, University of California, Santa Barbara, CA; **Ji Liu**, Argonne National Laboratory, Lemont, IL; **Hanrui Wang**, Song Han, Massachusetts Institute of Technology, Cambridge, MA

* Denotes a Best Paper Candidate

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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BEST MACHINE LEARNING SESSION IN- (RECENT)-MEMORY

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): In-memory and Near-memory Computing Architectures, Applications and Systems

Room: 3010, 3rd Floor

Session Chair(s): Laura Fick, Mythic; Biresh Kumar Joardar, Duke University

We've had a lot of good sessions on in-memory machine learning, but none as good as this one in recent memory. It is well known that Processing-in-memory (PIM) architectures are a promising choice for accelerating deep learning application with potentially orders of magnitude better performance. This session will present new PIM architectures that can be used for accelerating a wide variety of machine learning applications, including the latest transformers, random forest, and nearest neighbor search, along with ways to optimize them for even better performance.

LIGHTNING TALK – ADVANCES AND TRENDS ON ON-CHIP COMPUTE-IN-MEMORY MACROS AND ACCELERATORS

Jae-sun Seo, Arizona State University, Tempe, AZ

PROCESSING-IN-HIERARCHICAL-MEMORY ARCHITECTURE FOR BILLION-SCALE APPROXIMATE NEAREST NEIGHBOR SEARCH

Zhenhua Zhu, Jun Liu, Shulin Zeng, Huazhong Yang, Yu Wang, Tsinghua University, Beijing, China; Guohao Dai, Shanghai Jiao Tong University, Shanghai, China; Bing Li, Capital Normal University, Beijing, China

A DIGITAL 3D TCAM ACCELERATOR FOR THE INFERENCE PHASE OF RANDOM FOREST

Chieh-Lin Tsai, Tei-Wei Kuo, National Taiwan University, Taipei, Taiwan; Chun-Feng Wu, National Yang Ming Chiao Tung University, Hsinchu, Taiwan; Yuan-Hao Chang, Academia Sinica, Taipei, Taiwan; Han-Wen Hu, Macronix International Co., Ltd; National Tsinghua University, Hsinchu, Taiwan; Yung-Chun Lee, Hsiang-Pang Li, Macronix International Co., Ltd, Hsinchu, Taiwan

A CONVOLUTION NEURAL NETWORK ACCELERATOR DESIGN WITH WEIGHT MAPPING AND PIPELINE OPTIMIZATION

Lixia Han, Peng Huang, Zheng Zhou, Yiyang Chen, Xiaoyan Liu, Jinfeng Kang, Peking University, Beijing, China

HAIMA: A HYBRID SRAM AND DRAM ACCELERATOR-IN-MEMORY ARCHITECTURE FOR TRANSFORMER

Yan Ding, Chubo Liu, Mingxing Duan, Kenli Li, Hunan University, Changsha, China; Wanli Chang, University of York, United Kingdom; Keqin Li, State University of New York, New Paltz, NY

DEAR ACCELERATOR, COULD YOU PLEASE BE MORE SPECIFIC?

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): In-memory and Near-memory Computing Architectures, Applications and Systems

Room: 3003, 3rd Floor

Session Chair(s): Elaheh Sadredini, University of California, Riverside; Haitong Li, Purdue University

This session is on in-memory accelerators. The computing architectures leverage specialized hardware to improve the performance and energy efficiencies of applications within a specific domain. Across various domains, data-intensive workloads can greatly benefit from immersing computations into memories with architectural innovations offering application speedup and energy efficiency improvement. The session overviews the latest advancements in in-memory processing for genome graph analysis, algebraic multi-grid, and hardware security.

LIGHTNING TALK – IN-MEMORY & NEAR-MEMORY COMPUTING FOR “METAVERSE” APPLICATIONS: OPPORTUNITIES AND CHALLENGES

Huichu Liu, Meta, Menlo Park, CA

MEG2: IN-MEMORY ACCELERATION FOR GENOME GRAPHS ANALYSIS

Yu Huang, Long Zheng, Haifeng Liu, Zhuoran Zhou, Dan Chen, Pengcheng Yao, Qinggang Wang, Xiaofei Lao, Hai Jin, Huazhong University of Science and Technology, Wuhan, China

AMGR: ALGEBRAIC MULTIGRID ACCELERATED ON RERAM

Mingjia Fan, Xiaotian Tian, Junxian Li, Yiru Duan, Zhou Jin, Weifeng Liu, China University of Petroleum, Beijing, China; Yintao He, Ying Wang, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China; Xiaozhe Hu, Tufts University, Medford, MA

BP-NTT: FAST AND COMPACT IN-SRAM NUMBER THEORETIC TRANSFORM WITH BIT-PARALLEL MODULAR MULTIPLICATION

Jingyao Zhang, Elaheh Sadredini, University of California, Riverside, CA; Mohsen Imani, University of California, Irvine, CA

NTT-PIM: ROW-CENTRIC ARCHITECTURE AND MAPPING FOR EFFICIENT NUMBER-THEORETIC TRANSFORM ON PIM

Jaewoo Park, Sugil Lee, Jongeun Lee, UNIST, Ulsan, South Korea

Research Sessions

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RUNNING SOFTWARE ON EMBEDDED SYSTEMS: THEORY AND PRACTICE

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): Embedded System Design Methodologies

Room: 3008, 3rd Floor

Session Chair(s): Ihsen Alouani, Queen's University Belfast

The Embedded Systems Design Methodologies session includes four paper presentations, with contributions including efficient approaches to placement and scheduling of workloads on heterogeneous processors, leveraging stochastic search and by using Integer Linear Programming; as well as new theoretical results on worst-case execution time and response time for complex task graphs on embedded and heterogeneous processors.

LIGHTNING TALK – EFFICIENT EMBEDDED MACHINE LEARNING DEPLOYMENT ON EDGE AND IOT DEVICES

Sudeep Pasricha, Colorado State University, Fort Collins, CO

OMNIBOOST: BOOSTING THROUGHPUT OF HETEROGENEOUS EMBEDDED DEVICES UNDER MULTI-DNN WORKLOAD

Andreas Karatzas, Iraklis Anagnostopoulos, Southern Illinois University, Carbondale, IL

DMTSAR-ILP: ALLOCATING A UNIFIED DOMAIN PLATFORM FOR STREAMING APPLICATIONS

Bruno Morais, Gunar Schirner, Northeastern University, Boston, MA

ADAPTIVE: AGENT-BASED LEARNING FOR BOUNDING TIME IN MIXED-CRITICALITY SYSTEMS

Behnaz Ranjbar, Ali Hosseinghorban, **Akash Kumar**, Technische Universität Dresden, Germany

RESPONSE TIME ANALYSIS AND OPTIMIZATION OF DAG TASKS EXPLOITING MUTUALLY EXCLUSIVE EXECUTION

Haochun Liang, Xu Jiang, Northeastern University, Shenyang, China; Nan Guan, City University of Hong Kong; Qingqiang He, The Hong Kong Polytechnic University, Hong Kong; Wang Yi, Uppsala University, Uppsala, Sweden

UNLEASHING PRIVACY FOR AI

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Security/Privacy

Room: 3004, 3rd Floor

Session Chair(s): Benjamin Tan, University of Calgary

Navigating the challenges of AI and tremendous data and protecting privacy and intellectual property are the topics of this session. It focuses on the complex interplay between artificial intelligence (AI), large and complex data sets, and privacy. The session will present several interesting and exciting works that aim at building privacy-enhancing AI. Whether you are a business leader, data scientist, or privacy advocate, this session will provide valuable insights and practical solutions for ensuring that AI and data are used responsibly and in compliance with privacy. The session will delve into the latest advancements in privacy-enhancing methods and deep learning. The first paper, PASNet, presents a framework for secure two-party deep learning with low latency and high accuracy. The second paper, STML, focuses on secure IP for Tiny ML microcontrollers with optimized security and latency. The third paper proposes a new approach for privacy enhancement in machine learning using empirically-defined privacy evaluation. Finally, the fourth paper introduces Primer, a fast and accurate Transformer for NLP using encrypted data.

LIGHTNING TALK – PRIVATE AND SECURE LEARNING AT THE EDGE WITH HYPERDIMENSIONAL COMPUTING

Tajana Rosing, University of California, San Diego, CA

PASNET: POLYNOMIAL ARCHITECTURE SEARCH FRAMEWORK FOR TWO-PARTY COMPUTATION-BASED SECURE NEURAL NETWORK DEPLOYMENT

Hongwu Peng, Shanglin Zhou, Jiahui Zhao, Caiwen Ding, University of Connecticut, Storrs, CT; Yukui Luo, Shijin Duan, Xiaolin Xu, Northeastern University, Boston, MA; Nuo Xu, Ran Ran, Wujie Wen, Lehigh University, Bethlehem, PA; Chenghong Wang, Duke University, Durham, NC; Tong Geng, University of Rochester, Rochester, NY

IP PROTECTION IN TINY ML

Jinwen Wang, Yuhao Wu, Han Liu, Roger Chamberlain, **Ning Zhang**, Washington University, St. Louis, MO; Bo Yuan, Rutgers University, Piscataway Township, NJ

\mathbb{Z}_2 : CRYPTO-CLEAR PRIVATE INFERENCE

Yuke Zhang, Dake Chen, Haomei Liu, Ruiheng Peng, Peter Beerel, University of Southern California, Los Angeles, CA; Souvik Kundu, Intel, San Diego, CA

PRIMER: A PRIVACY-PRESERVING TRANSFORMER ON ENCRYPTED DATA

Mengxin Zheng, Lei Jiang, Indiana University, Bloomington, IN; Qian Lou, University of Central Florida, Orlando, FL

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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WHY IS CURVY DESIGN AN OPPORTUNITY NOW?

Time: 1:30 PM – 3:00 PM

Event Type: Research Panel

Topic Area(s): EDA, Design

Room: 3014, 3rd Floor

Organizer(s): Jan Willis, Calibra Consulting, Menlo Park, CA;

There is an opportunity to take advantage of what semiconductor manufacturing has enabled for the first time in 40 years - a wholesale change in what future chips could look like by manufacturing curvilinear features. Curvy designs would yield better, use less power, decrease chip size and have better performance yield, too. But most of the chip design community isn't yet aware that curvilinear manufacturing is now possible. No doubt there are several controversial aspects to this topic: a) the economics of curvy design, b) organizational dynamics of the design-to-manufacturing handoff, c) what EDA tools will need to be rewritten, and d) how will large data volumes be managed. This session is about bridging that awareness from manufacturing to the design community and providing insights on the areas of controversy.

The moderator will open the session by summarizing capabilities that exist today for curvilinear manufacturing, areas where EDA tools can or must change, and work already in place to address data volumes. Each panelist will provide their unique view on the benefits of curvy design and one or more perceived barriers. It will take time and investment from both design and EDA experts as well as corporate and product development business leaders to take advantage of what semiconductor manufacturing has enabled for the first time in 40 years. Our goal is to explain why manufacturing is no longer a barrier to curvy design, spark the imagination of the EDA and design community about the benefits and debate the challenges beyond manufacturing to make curvy design a reality.

The moderator will open the session by summarizing capabilities that exist today for curvilinear manufacturing, areas where EDA tools can or must change, and work already in place to address data volumes. Each panelist will provide their unique view on the benefits of curvy design and one or more perceived barriers. It will take time and investment from both design and EDA experts as well as corporate and product development business leaders to take advantage of what semiconductor manufacturing has enabled for the first time in 40 years. Our goal is to explain why manufacturing is no longer a barrier to curvy design, spark the imagination of the EDA and design community about the benefits and debate the challenges beyond manufacturing to make curvy design a reality.

Moderator: Aki Fujimura, D2S, Saratoga, CA

Panelists: Steve Teig, Perceive, San Jose, CA; Ezequiel Russell, Micron, Boise, ID; John Kibarian, PDF Solutions Inc., Santa Clara, CA; Andrew Kahng, UC San Diego

ALGORITHMS, ARCHITECTURE, CIRCUITS, AND DEVICES FOR GENOME SEQUENCING ACCELERATION

Time: 1:30 PM – 3:00 PM

Event Type: Special Session (Research)

Topic Area(s): Embedded Systems

Room: 3001, 3rd Floor

Organizer(s): Preeti Ranjan Panda, Indian Institute of Technology, Delhi

Genome analysis is critical for many important scientific, medical, and societal reasons, including personalized medicine, outbreak detection, evolutionary understanding, and discoveries. Modern genome sequencing technologies are capable of generating unprecedented amounts of genomic data at high speed and very low cost. Unfortunately, modern computing systems used for genomic data analysis are unable to cope with such data since they are not specialized for processing genomic data and are overwhelmed by data movement. There is a dire need for developing complete systems for efficient, high-performance, and intelligent genomic data analysis.

In this special session, we motivate the need for domain-specific computing in the sequencing field. The attendees at DAC comprise experts in algorithms, architectures, circuits, and devices, and automating designs at these various levels of abstraction. These specialists, the attending students, and early career researchers can contribute significantly to the research and development in the emerging area of Genomic Sequencing Acceleration. The session comprises of three talks: the first talk will motivate the need for the Acceleration of Genome sequence analysis and then continue to explain some of the early architectures utilized and their limitations; the second talk will discuss how Genome analysis can be sped up by the use of Algorithm Architecture Co-design; and the last talk will discuss the latest sequencers, the long reads which emerge from them, and architectures to speed up their analysis.

THE ALGORITHMS AND THE NEED FOR NOVEL ARCHITECTURES AND ACCELERATION FOR GENOME SEQUENCE ANALYSIS

Sri Parameswaran, University of New South Wales, Sydney, Australia

ACCELERATING GENOME ANALYSIS VIA ALGORITHM-ARCHITECTURE CO-DESIGN

Onur Mutlu, ETH Zürich, Zurich, Switzerland

NOVEL ALGORITHMS AND ARCHITECTURES FOR LONG READ SEQUENCE ANALYSIS

Hasindu Gamaarachchi, University of New South Wales, Sydney, Australia

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

DESIGN CONSIDERATIONS AND TRADEOFFS FOR 2.5D CHIPLET SOLUTIONS

Time: 2:00 PM – 2:45 PM

Event Type: DAC Pavilion Panel

Topic Area(s): Design

Room: DAC Pavilion, Level 2 Exhibit Hall

The interest in chiplets has increased dramatically to expand performance, mitigate rising mask costs, and enable reuse. Initially, chiplets, 2.5D, and 3D solutions were reserved for the knighted few, Intel with its Foveros technology, AMD's CCD for its Zen CPU line, and Broadcom with its Spectrum-4. Now, mid- and small-cap companies alike are targeting chiplets for economic and performance reasons. This panel will examine and discuss product decisions, such as die-to-die interface technology, packaging considerations, and verification methodologies through EDA, hyperscaler, clocking, and packaging lens. Before entering the panel discussion, the moderator will provide the audience with a brief history of 2.5D and D2D solutions while defining key terms to provide level grounding for the audience. The panel will discuss:

- What factors are driving 2.5D adoption? How is this adoption changing your segment?
- What tools, flow, methodology, and architectural considerations are required for modern 2.5D designs?
- What are the tradeoffs for system designers to consider when comparing BoW vs. UCle vs. other solutions? What applications best suited for each technology?

The panel will end with forward-looking statements on the future of 2.5D and 3D solutions. The panelists will explore possible improvements in methodology, tools, and technology.

Moderator: Ed Sperling, Semiconductor Engineering, San Jose, CA

Panelists: Saif Alam, Movellus; Craig Bishop, Deca Technologies; Mark Kuemerle, Marvell; Tony Mastroianni, Siemens EDA

INCREASE THROUGHPUT AND PRODUCTIVITY WITH CADENCE TOOLS IN THE CLOUD USING FLEXIBLE AWS COMPUTE CHOICES

Time: 2:45 PM – 5:45 PM

Event Type: Hands-On Training Session

Topic Area(s): Cloud

Room: Level 2 Foyer

With the variety of EDA tools required to deliver a modern design, optimizing time to results for each workload can lead to better coverage and increased engineering productivity. However, some EDA workloads require faster CPUs, some require larger L3 cache, while others depend on the RAM/core ratio. Using AWS, customers can find the optimal compute options to run their Cadence tools. In this hands-on workshop we learn how to find the right compute option for your Cadence tool, and learn how R&D can optimize their design and verification processes by proactively choosing the type of HPC hosts used to run Cadence workloads in AWS. Each user will benchmark multiple compute types and learn how to calculate cost/performance trade-offs for their own workload.

Presenter: Eran Brown, Sr. Semiconductor Solutions Architect, AWS

Co-presenter: Eamon O’Gorman, Business Development Director, Cadence

ASK ME ANYTHING WITH JOE COSTELLO AND WALLY RHINES

Time: 3:00 PM – 3:45 PM

Event Type: DAC Pavilion Panel

Topic Area(s): EDA

Room: DAC Pavilion, Level 2 Exhibit Hall

In the EDA industry’s long, storied history, Joseph Costello and Walden C. Rhines stand as two of the most influential executives we’ve seen. Now, the former CEOs of Cadence and Mentor join together again in a special event – a live Ask me Anything. Whether you’re an industry vet or fresh from college, you’ll have the opportunity to talk to two men who not only grew their companies but leveraged their passion, vision and their intellect to grow the EDA business at the same time. Remember Wally’s Sunday forecast presentations, those master classes in how to use data and wit to tell powerful stories? Remember Joe’s legendary dog bowl reference or any extemporaneous speech about the industry and its future? You could hear a pin drop when he took the stage. Here’s your opportunity to ask two legendary, engaging industry figures questions about the past, present and future of the most vital innovation ecosystem the world has ever known.

Moderator: Brian Fuller, Arm Ltd., San Jose, CA

Panelists: Joe Costello, Metrics, Kwikbit, Arrikto, Acromove, Berkeley, CA; Walden Rhines, Cornami, Inc., Dallas, TX

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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THE NEXT FRONTIERS IN THE FRONT END

Time: 3:30 PM – 5:00 PM

Event Type: Engineering Tracks

Topic Area(s): Front-End Design

Room: 2010, 2nd Floor

Session Chair(s): Ankit Gopani, Intel

Emergence of AI has fueled an arms race to design new kinds of hardware to run them optimally and that in turn is accelerating innovation in design and verification methodologies. Come and learn the latest industry trends in front-end design – from machine learning based CDC to high level synthesis to LLVM compilers for RISC-V.

CLASSIFICATION OF CLOCK DOMAIN CROSSING (CDC) DATA USING MACHINE LEARNING

Suhyun Yun, Youngchan Lee, Woojoo Space, Kunhyuk Kang, Samsung Electronics, Hwaseong, South Korea; Varun Sharma, Vikas Sachdeva, Real Intent Inc, Bangalore, India; Hyobeon Park, Real Intent Inc, Sunnyvale, CA

RE-TARGETABLE C/C++ LLVM COMPILER FOR RISC-V

Zdeněk Přikryl, Codasip, Brno, Czech Republic

EFFORTLESS DSP EXTENSIONS DESIGN FOR EMBEDDED RISC-V CORES

Ettore Giliberti, Codasip, Barcelona, Spain; Alexey Shchekin, Codasip, Munich, Germany

SPEEDING-UP RISC-V GPGPU ACCELERATOR USING HIGH-BANDWIDTH MEMORY ON FPGA

Blaise Tine, Hyesoon Kim, Georgia Institute of Technology, Atlanta, GA

HIGH LEVEL SYNTHESIS FOR SEQUENTIAL NESTED LOOPS: FULLY HARDWIRED SLAM LOCAL BUNDLE ADJUSTMENT

Atsushi Hatabu, Toshihiko Nakamura, NEC Corporation, Kawasaki, Japan; Kenichi Miyazaki, MIRISE Technologies Corporation, Nisshin, Japan; Kazutoshi Wakabayashi, The University of Tokyo, Japan

WHY THE DELAY? ENABLING TIME

Time: 3:30 PM – 5:00 PM

Event Type: Engineering Tracks

Topic Area(s): Back-End Design

Room: 2008, Level 2

Session Chair(s): Patricia Fong, Marvell Semiconductor

Time never stops for anyone. Take quick bites of wisdom from the Time travelers to speed forward through to get closure and peace of mind. All the latest from the mobius loop!

AN EFFICIENT AND COST-EFFECTIVE METHOD TO DETECT AND ANALYZE ESD CDM RISKS IN DESIGNS

Subhadeep Ghosh, Texas Instruments, Karnataka, India; Kaustav Ray, Texas Instruments, Bangalore, India; Raj Sankaralingam, Texas Instruments, Dallas, TX; Rith Pok, Texas Instruments, Plano, TX

A NOVEL SOLUTION FOR 3NM/4NM AND BELOW LVS CHALLENGES: LOCAL LAYOUT EFFECTS EXTRACTION QA IN LVS RULE DECK

Jaeyoung So, Jimin Yeo, Jongku Kang, Heejae Lim, Yongseok Lee, Minh Jung, Younggrog Jo, Samsung Electronics, Hwaseong, South Korea; **Ahmed Saleh**, Siemens EDA, Richmond, VA; Mohamed Alimam, Siemens EDA, Tokyo, Japan

DESIGN DATA BROWSER (DDB) A HIGH-PERFORMANCE INTERACTIVE ENVIRONMENT FOR TIMING TRIAGE

Kerim Kalafala, IBM, Hopewell Junction, NY; Robert Allen, IBM, San Jose, CA; Deb Dean, IBM, Cary, NC; Mitch DeHond, IBM, Williston, ND; Nate Hieter, Rich Taggart, Chris Cavitt, IBM, Poughkeepsie, NY; Ed Hughes, IBM, Blue Bell, PA; Doug Keller, IBM, Houston, TX; Anurag Kompalli, IBM, East Lansing, MI

AGING-AWARE STATIC TIMING ANALYSIS WITH TIMING ARC-LEVEL MODELING

Jingon Lee, Samsung Electronics, Hwaseong, South Korea; Sangwoo Han, Synopsys, San Francisco, CA; Li Ding, Synopsys, San Jose, CA, Ruijing Shen, Synopsys, New York City, NY

PREDICTIVE CROSSTALK FIXING USING XGBOOST REGRESSOR

Anmol Khatri, Intel, Rajasthan, India; Aniket Agrawal, Intel, Karnataka, India; Lalit Arora, Intel, Delhi, India; Praveen Chinta, Intel Corporation India; Soumik Mukherjee, Intel Corporation India; **Andy Li**, Intel Corporation, US

TURNAROUND TIME/COMPUTE REDUCTION FOR 3DIC TIMING SIGNOFF

Tusharkant Mishra, Samsung Semiconductor, Bangalore, India; Mijeong Lim, **Ki-Ok Kim**, Samsung Electronics, Hwaseong, South Korea; Ranjith V R, Samsung Electronics, Kerala, India

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

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CROSS-LAYER COMPUTE-IN-MEMORY BEYOND MACHINE LEARNING: CIRCUIT, ARCHITECTURE, EDA

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): In-memory and Near-memory Computing Circuits and Architectures

Room: 3010, 3rd Floor

Session Chair(s): Rangharajan Venkatesan, NVIDIA; Wenfeng Zhao, Binghamton University

The demand for accelerated computing is going exponentially from machine learning to emerging non-machine learning applications. Compute-in-Memory (CIM) offers us a promising path to improving computing performance but needs to rely on collaborative circuit/architecture innovations as well as efficient software stack to unleash its true potential. This session presents six research papers focusing on design innovations across circuit, architecture, and software to accelerate emerging computing problems in genomics, communication, and electronic design automation.

LIGHTNING TALK – CROSS-LAYER COMPUTE-IN-MEMORY BEYOND MACHINE LEARNING: CIRCUIT, ARCHITECTURE, EDA IN-MEMORY COMPUTING ACROSS THE STACK - VIRTUES, MYTHS, AND HALF-TRUTHS

Naveen Verma, Princeton University, Princeton, NJ

ASMCAP: AN APPROXIMATE STRING MATCHING ACCELERATOR FOR GENOME SEQUENCE ANALYSIS BASED ON CAPACITIVE CONTENT ADDRESSABLE MEMORY

Hongtao Zhong, Zhonghao Chen, Chen Wang; Yongpan Liu, Huazhong Yang, Xueqing Li, Tsinghua University, Beijing, China; Wenqin Huangfu, University of California, Santa Barbara, CA; Tianyi Wang, Yao Yu, Daimler Greater China Ltd., Beijing, China; Yixin Xu, Vijaykrishnan Narayanan, Pennsylvania State University, University Park, PA

VICTOR: A VARIATION-RESILIENT APPROACH USING CELL-CLUSTERED CHARGE-DOMAIN COMPUTING FOR HIGH-DENSITY HIGH-THROUGHPUT MLC CIM

Mingyen Lee, Wenjun Tang, Yiming Chen, Juejian Wu, Hongtao Zhong, Yongpan Liu, Huazhong Yang, Xueqing Li, Tsinghua University, Beijing, China; Yixin Xu, Vijaykrishnan Narayanan, Penn State University, State College, PA

FSPA: AN FEFET-BASED SPARSE MATRIX-DENSE VECTOR MULTIPLICATION ACCELERATOR

Xiaoyu Zhang, Zerun Li, Rui Liu, Xiaoming Chen, Yinhe Hah, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

AUTODCIM: AN AUTOMATED DIGITAL CIM COMPILER

Jia Chen, Fengbin Tu, Kunming Shao, Fengshi Tian, Xiao Huo, Chi Ying Tsui, Tim Cheng, Hong Kong University of Science and Technology, Hong Kong

DSPIMM: DIGITAL SPARSE IN-MEMORY MATRIX VECTOR MULTIPLIER FOR COMMUNICATION APPLICATIONS

Amitesh Sridharan, Fan Zhang, Deliang Fan, Arizona State University, Tempe, AZ; Yang Sui, Bo Yuan, Rutgers University, Piscataway Township, NJ

UPPIPE: A NOVEL PIPELINE MANAGEMENT ON IN-MEMORY PROCESSORS FOR RNA-SEQ QUANTIFICATION

Liang-Chi Chen, Chien-Chung Ho, National Cheng Kung University, Tainan, Taiwan; Yuan-Hao Chang, Academia Sinica, Taipei, Taiwan

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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GOT AN ACRONYM? BUILDING SECURE ARCHITECTURES AND ACCELERATORS

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Hardware Security: Primitives, Architecture, Design & Test

Room: 3012, 3rd Floor

Session Chair(s): Vikram Suresh, SquareUp; Hamed Okhravi, Massachusetts Institute of Technology

Security researchers love to create acronyms. Each of the six papers in this session has one as the authors build secure architectures and hardware-based accelerators. DriverJar utilizes hardware watchpoint to achieve driver isolation for ARM-based devices. EP-ORAM is an efficient and NVM-friendly path eviction scheme to mitigate the high DRAM demand in ring ORAM. PIMA-LPN accelerates the computation of learning parity with noise by processing-in-memory. Mkeycutter is an FPGA-based accelerator for the McEliece quantum-resistant public-key scheme. CHAM is another FPGA-based accelerator for matrix-vector product in homomorphic encryption. AccShield enhances trusted execution environments to cloud for the secure computation of machine learning TPU accelerators.

LIGHTNING TALK – GOT AN ACRONYM? BUILDING SECURE ARCHITECTURES AND ACCELERATORS PROCESSOR VULNERABILITY DISCOVERY

Yongqiang Lyu, Tsinghua University, Beijing, China

DRIVERJAR: LIGHTWEIGHT DEVICE DRIVER ISOLATION FOR ARM

Huamao Wu, Yuan Chen, **Yajin Zhou**, Zhejiang University, Hangzhou, China; Yifei Wang, Lubo Zhang, Huawei, Beijing, China

EP-ORAM: EFFICIENT NVM-FRIENDLY PATH EVICTION FOR RING ORAM IN HYBRID MEMORY

Mehrnoosh Raoufi, Jun Yang, Xulong Tang, Youtao Zhang, University of Pittsburgh, PA

PIMA-LPN: PROCESSING-IN-MEMORY ACCELERATION FOR EFFICIENT LPN-BASED POST-QUANTUM CRYPTOGRAPHY

Lin Ding, Jiliang Zhang, Hunan University, Changsha, China; Song Bian, Beihang University, Beijing, China

MKEYCUTTER: A HIGH-THROUGHPUT KEY GENERATOR OF CLASSIC MCELIECE ON HARDWARE

Yihong Zhu, Wenping Zhu, Chen Chen, Zhengdong Li, Shaojun Wei, Leibo Lu, Tsinghua University, Beijing, China; Min Zhu, Wuxi Micro Innovation Integrated Circuit Design Co.Ltd, Wuxi, China

CHAM: A CUSTOMIZED HOMOMORPHIC ENCRYPTION ACCELERATOR FOR FAST MATRIX-VECTOR PRODUCT

Xuanle Ren, **Zhaohui Chen**, Zhen Gu, Yanheng Lu, Ruiguang Zhong, Wen-jie Lu, Jiansong Zhang, Yichi Zhang, Heng Liu, Cheng Hong, Alibaba Group, Beijing, China; Hanghang Wu, Xiaofu Zheng, Tingqiang Chu, Changzheng Wei, Ant Finance, Shanghai, China; Dimin Niu, Yuan Xie, Alibaba Group, Sunnyvale, CA

ACCSHIELD: A NEW TRUSTED EXECUTION ENVIRONMENT WITH MACHINE-LEARNING ACCELERATORS

Wei Ren, William Kozlowski, Deming Chen, University of Illinois at Urbana-Champaign, Urbana, IL; Sandhya Koteswara, Mengmei Ye, Hubertus Franke, IBM Thomas J. Watson Research Center, Yorktown Heights, NY

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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LET'S GO FAST – DNN ACCELERATION!

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Architecture Design

Room: 3003, 3rd Floor

Session Chair(s): Hyoukjun Kwon, University of California, Irvine; Priya Panda, Yale University

DNN acceleration finds its way for efficiency. In this session, DNN acceleration architectures are examined with DPU, RISC-V and Optical DNN, and the acceleration energy efficiency is investigated with point cloud neural networks.

LIGHTNING TALK – LET'S GO FAST – DNN ACCELERATION EFFICIENCY AND PROGRAMMABILITY OF DNN ACCELERATORS AND GPUS!

Won Woo Ro, Yonsei University, Seoul, South Korea

FIONA: FINE-GRAINED INCOHERENT OPTICAL DNN ACCELERATOR SEARCH TOWARDS SUPERIOR EFFICIENCY AND ROBUSTNESS

Mengquan Li, Kenli Li, Mingfeng Lan, Jie Xiong, Zhuo Tang, Hunan University, Changsha, China; Weichen Liu, Nanyang Technological University, Singapore

ACCELERATING DNN INFERENCE WITH HETEROGENEOUS MULTI-DPU ENGINES

Zelin Du, **Wei Zhang**, Zimeng Zhou, Lei Ju, Shandong University, Qingdao, China; Zili Shao, The Chinese University of Hong Kong, Shatin, Hong Kong

FLNA: AN ENERGY-EFFICIENT POINT CLOUD FEATURE LEARNING ACCELERATOR WITH DATAFLOW DECOUPLING

Dongxu Lyu, Zhenyu Li, Yuzhou Chen, Ningyi Xu, Guanghui He, Shanghai Jiao Tong University, Shanghai, China

AN EFFICIENT ACCELERATOR FOR POINT-BASED AND VOXEL-BASED POINT CLOUD NEURAL NETWORKS

Xinhao Yang, Tianyu Fu, Shulin Zeng, Kai Zhong, Ke Hong, Yu Wang, Tsinghua University, Beijing, China; Guohao Dai, Shanghai Jiao Tong University, Shanghai, China

ADAS: A FAST AND ENERGY-EFFICIENT CNN ACCELERATOR EXPLOITING BIT-SPARSITY

Xiaolong Lin, Gang Li, Zizhao Liu; Zhuoran Song, Naifeng Jing, Xiaoyao Liang, Shanghai Jiao Tong University, Shanghai, China; Yadong Liu, Fan Zhang, Alibaba Group, Hangzhou, China

DBPS: DYNAMIC BLOCK SIZE AND PRECISION SCALING FOR EFFICIENT DNN TRAINING SUPPORTED BY RISC-V ISA EXTENSIONS

Seunghyun Lee, Jeik Choi, Seock-Hwan Noh, Jahyun Koo, Jaeha Kung, Daegu Gyeongbuk Institute of Science and Technology, Dalseong-gun, South Korea

MAKING AI SMARTER, FASTER, AND MORE EFFICIENT

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Algorithms

Room: 3004, 3rd Floor

Session Chair(s): Tianqi Tang, Meta; Zhuoran Zhao, Facebook

Real-life application scenarios raise three important demands on AI algorithms: higher accuracy (smarter), rapid development (faster), and lower resource overhead (more efficient). The presentations in this session provide in-depth solutions for these targets, including five papers with various optimizations for EDA-driven learning, knowledge distillation, transfer learning, neural architecture search, and mixed-precision quantization.

LIGHTNING TALK – “MAKING AI SMARTER, FASTER, AND MORE EFFICIENT”: CURRENT APPROACHES AND LOOKING INTO THE FUTURE

Yingyan (Celine) Lin, Georgia Institute of Technology, Atlanta, GA

ON EDA-DRIVEN LEARNING FOR SAT SOLVING

Min Li, **Zhengyuan Shi**, Qiuxia Lai, Sadaf Khan, Qiang Xu, The Chinese University of Hong Kong, Hong Kong; Shaowei Cai, University of Chinese Academy of Sciences, Beijing, China

IFHE: INTERMEDIATE-FEATURE HETEROGENEITY ENHANCEMENT FOR IMAGE SYNTHESIS IN DATA-FREE KNOWLEDGE DISTILLATION

Yi Chen, Ao Ren, Tao Yang, Duo Liu, Chongqing University, Chongqing, China; Ning Liu, Midea Group, Beijing, China

ROBUST TICKETS CAN TRANSFER BETTER: DRAWING MORE TRANSFERABLE SUBNETWORKS IN TRANSFER LEARNING

Yonggan Fu, Shang Wu, Yingyan (Celine) Lin, Georgia Institute of Technology, Atlanta, GA; Ye Yuan, University of California, Santa Barbara, CA; Jiayi Yuan, Rice University, Houston, TX

PERTNAS: ARCHITECTURAL PERTURBATIONS FOR MEMORY-EFFICIENT NEURAL ARCHITECTURE SEARCH

Afzal Ahmad, Zhiyao Xie, Wei Zhang, Hong Kong University of Science and Technology, Hong Kong

CSQ: GROWING MIXED-PRECISION QUANTIZATION SCHEME WITH BI-LEVEL CONTINUOUS SPARSIFICATION

Lirui Xiao, Li Du, Nanjing University, Nanjing, China; **Huanrui Yang**, Zhen Dong, Kurt Keutzer, University of California, Berkeley, CA; Shanghang Zhang, Peking University, Beijing, China

Research Sessions

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MULTI-ACCELERATOR AND DISTRIBUTED SYSTEM FOR ML

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML System and Platform Design

Room: 3006, 3rd Floor

Session Chair(s): Meng Li, Facebook

As AI and machine learning models become increasingly complex, the need for employing a distributed system or multiple accelerators with efficient communication mechanisms becomes more critical. This session presents the latest innovations to meet these demands for high-performance ML systems. It features four papers that introduce novel AI/ML frameworks for effectively mapping workloads to accelerators for different ML methods, one paper discussing the use of CGRA for ML acceleration, and another paper detailing an AXI-compliant NoC design for a multi-accelerator system.

LIGHTNING TALK – MULTI-ACCELERATOR AND DISTRIBUTED SYSTEM FOR ML

Muhammad Shafique, University of New York, Abu Dhabi, UAE

PATRONOC: PARALLEL AXI TRANSPORT REDUCING OVERHEAD FOR NETWORK-ON-CHIPS TARGETING MULTI-ACCELERATOR DNN PLATFORMS AT THE EDGE

Vikram Jain, Marian Verhelst, KU Leuven, Belgium; **Matheus Cavalcante**, Michael Rogenmoser, Thomas Benz, Andreas Kurth, ETH Zürich, Switzerland; Nazareno Bruschi, Davide Rossi, Luca Benini, University of Bologna, Italy

ADAGL: ADAPTIVE LEARNING FOR AGILE DISTRIBUTED TRAINING OF GIGANTIC GNNS

Ruisi Zhang, Mojan Javaheripi, Farinaz Koushanfar, University of California, San Diego, CA; Zahra Ghodsi, Purdue University, Lafayette, IN; Amit Bleiweiss, Intel, Haifa, Israel

ML-CGRA: AN INTEGRATED COMPILATION FRAMEWORK TO ENABLE EFFICIENT MACHINE LEARNING ACCELERATION ON CGRAS

Yixuan Luo, Tong Geng, University of Rochester, Rochester, NY; Cheng Tan, Nirav Dave, Microsoft, New York, NY; **Nicolas Bohm Agostini**, Northeastern University, Boston, MA; Ang Li, Antonino Tumeo, Pacific Northwest National Laboratory, Richland, WA

MIXPIPE: EFFICIENT BIDIRECTIONAL PIPELINE PARALLELISM FOR TRAINING LARGE-SCALE MODELS

Weigang Zhang, Biyu Zhou, Xuehai Tang, Zhaoxing Wang, Songlin Hu, Institute of Information Engineering, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

MARS: EXPLOITING MULTI-LEVEL PARALLELISM FOR DNN WORKLOADS ON ADAPTIVE MULTI-ACCELERATOR SYSTEMS

Guan Shen, Jieru Zhao, Chentao Wu, Quan Chen, Minyi Guo, Shanghai Jiao Tong University, Shanghai, China; Zeke Wang, Zhejiang University, Hangzhou, China; Zhe Lin, Peng Cheng Laboratory, Shenzhen, China; Wenchao Ding, Huawei, Shanghai, China

RESPECT: REINFORCEMENT LEARNING BASED EDGE SCHEDULING ON PIPELINED CORAL EDGE TPUS

Jiaqi Yin, Yingjie Li, Daniel Robinson, Cunxi Yu, University of Utah, Salt Lake City, UT

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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NOVEL TECHNIQUES IN SYNTHESIS AND VERIFICATION OF ANALOG CIRCUITS

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Analog CAD, Simulation, Verification and Test

Room: 3002, 3rd Floor

Session Chair(s): Markus Olbrich, Leibniz University Hannover; Arvind Sharma, imec

The session covers multiple approaches using Voronoi trees and reinforcement learning, multiagent and gm/ID based methods to tackle the synthesis problem. The addressed applications are transistor-level circuit design, hierarchical block level analog systems, electronics of flat panels up to microstrip transmission lines. Verification papers present solutions to decrease run times for large-scale circuit simulation tasks by substantial improving matrix handling with respect to their density and structure.

LIGHTNING TALK – NOVEL TECHNIQUES IN SYNTHESIS AND VERIFICATION OF ANALOG CIRCUITS

Georges Gielen, KU Leuven, Belgium

CVTS: A CONSTRAINED VORONOI TREE SEARCH METHOD FOR HIGH DIMENSIONAL ANALOG CIRCUIT SYNTHESIS

Aidong Zhao, Fudan University, Shanghai, China; Xianan Wang, Dian Zhou, The University of Texas at Dallas, Richardson, TX; Zixiao Lin, University of California, San Diego, CA; **Zhaori Bi**, Xudong Li, Changhao Yan, Fan Yang, Li Shang, Xuan Zeng, Fudan University, Shanghai, China

REINFORCEMENT LEARNING-BASED ANALOG CIRCUIT OPTIMIZER USING GM/ID FOR SIZING

Minjeong Choi, Samsung Advanced Institute of Technology, Gyeonggi-do, South Korea; Youngchang Choi, Kyongsu Lee, Seokhyeong Kang, Pohang University of Science and Technology, Pohang, South Korea

AUTOMATED DESIGN OF COMPLEX ANALOG CIRCUITS WITH MULTIAGENT BASED REINFORCEMENT LEARNING

Jinxin Zhang, Jiarui Bao, Zhangcheng Huang, Xuan Zeng, **Ye Lu**, Fudan University, Shanghai, China

MTL-DESIGNER: AN INTEGRATED FLOW FOR ANALYSIS AND SYNTHESIS OF MICROSTRIP TRANSMISSION LINE

Qipan Wang, Yibo Lin, Runsheng Wang, Ru Huang, Peking University, Beijing, China; Ping Liu, Liguang Jiang, Xpedic, Shanghai, China; Mingjie Liu, NVIDIA, Austin, TX

FPDSIM: A STRUCTURAL SIMULATOR FOR POWER GRID ANALYSIS OF FLAT PANEL DISPLAY

Chengtao An, Chunqiao Li, Yangfeng Su, Fan Yang, Xuan Zeng, Fudan University, Shanghai, China; Xiangqi Li, Emphyrean Technology, Beijing, China

ACCELERATING SPARSE LU FACTORIZATION WITH DENSITY-AWARE ADAPTIVE MATRIX MULTIPLICATION FOR CIRCUIT SIMULATION

Tengcheng Wang, Wenhao Li; Haojie Pei, Yuying Sun, **Zhou Jin**, Weifeng Liu, China University of Petroleum, Beijing, China

ROUTE ME IF YOU CAN!

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Physical Design and Verification

Room: 3008, 3rd Floor

Session Chair(s): Jinwei Liu, The Chinese University of Hong Kong; Vidya Chhabria, Arizona State University

We journey through advances in routing algorithms spanning PCB, chiplet, and ASIC. First, we visit PCB routing with a highly efficient algorithm handling multiple design rules and algorithms for solving the escape and bus routing problems. Next, we meet a novel algorithm that solves the any-angle multi-redistribution routing problem for chiplets. Then, a highly efficient directed acyclic graph-based routing algorithm will be introduced. The fifth work takes a fresh look at solving the routing problem via an ILP Lagrangian relaxation and a direction-aware A* algorithm. The final work presents OpenDRC, a GPU-accelerated design rule checker.

LIGHTNING TALK – FEASIBILITY CHECKING FOR ADVANCED PACKAGING

Wen-Hao Liu, Cadence Design Systems, Inc., San Francisco, CA

A MATCHING BASED ESCAPE ROUTING ALGORITHM WITH VARIABLE DESIGN RULES AND CONSTRAINTS

Qinghai Liu, **Disi Lin**, Chuandong Chen, Fuzhou University, Fuzhou, China; Huan He, Hangzhou Huawei Enterprises Telecommunication Technologies Co., LTD, Hangzhou, China; Jianli Chen, Fudan University, Shanghai, China; Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

DISJOINT-PATH AND GOLDEN-PIN BASED IRREGULAR PCB ROUTING WITH COMPLEX CONSTRAINTS

Qinghai Liu, **Qinfei Tang**, Jiarui Chen, Chuandong Chen, Fuzhou University, Fuzhou, China; Ziran Zhu, Southeast University, Nanjing, China; Huan He, Hangzhou Huawei Enterprises Telecommunication Technologies Co., LTD, Hangzhou, China; Jianli Chen, Fudan University, Shanghai, China; Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

ANY-ANGLE ROUTING FOR REDISTRIBUTION LAYERS IN 2.5D IC PACKAGES

Min-Hsuan Chung, Je-Wei Chuang, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

EDGE: EFFICIENT DAG-BASED GLOBAL ROUTING ENGINE

Jinwei Liu, Evangeline Young, The Chinese University of Hong Kong, Hong Kong

PATHFINDING MODEL AND LAGRANGIAN-BASED GLOBAL ROUTING

Pengju Yao, Ping Zhang, Wenxing Zhu, Fuzhou University, Fuzhou, China

OPENDRC: AN EFFICIENT OPEN-SOURCE DESIGN RULE CHECKING ENGINE WITH HIERARCHICAL GPU ACCELERATION

Zhuolun He, Bei Yu, The Chinese University of Hong Kong; Yihang Zuo, Jiayi Jiang, Haisheng Zheng, Shanghai Artificial Intelligence Laboratory, Shanghai, China; Yuzhe Ma, The Hong Kong University of Science and Technology, Guangzhou, China

Research Sessions

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Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

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Engineering Track

CHIPS & SCIENCE & EDA: A NEW (AND AMPLIFIED) FUTURE?

Time: 3:30 PM – 5:30 PM

Event Type: Research Panel

Topic Area(s): EDA

Room: 3014, 3rd Floor

Organizer: Rob Rutenbar, University of Pittsburgh, Pittsburgh, PA

We are witnessing a remarkable global resurgence of interest in semiconductors and related technologies. These have emerged as key components of both national security and economic stability. In the US, the CHIPS and Science Act of 2022 provides over \$250B to boost US research and manufacturing in this arena. And the US is not alone here. The European Commission has proposed a European Chips Act to invest in these same technologies. Prominent semiconductor foundries and verticals are building new fabs in new geographies and promising easier access to leading-edge technologies for academics and other researchers. So – how does this affect the DAC community? We are an extremely broad community: global academics, aspiring entrepreneurs, rising startups, established commercial players. What new resources and technologies might be available to researchers? To startups? To commercial enterprises already established as part of the semiconductor supply chain? How are government and corporate sponsors collaborating? And, given the somewhat complex geopolitics underlying some of these investments, what does this mean for international collaborations? How is this pivot viewed in different parts of the globe? Our panelists include leadership from the organizations on the frontlines of deciding how the technical community will respond in this brave new world. Leaders from NIST, NSF, DARPA, SRC, IMEC, TSMC and the venture community, will share their perspectives and plans, for this eventful new era.

Moderator: Rob Rutenbar, University of Pittsburgh, Pittsburgh, PA

Panelists: Margaret Martonosi, National Science Foundation, New York, NY; Carl McCants, DARPA, Arlington, VA; Todd Younkin, Semiconductor Research Corporation, Raleigh, NC; Laurie Locascio, National Institute of Standards and Technology, Gaithersburg, MD; Max (Masoud) Mirgoli, imec, San Francisco, CA; Nicholas Montella, TSMC, Washington, DC; Arash Afrakhteh, Pear VC, Menlo Park, CA

CLOUD AND EDGE: NEW AGE OF AUTOMOTIVE COMPUTING

Time: 3:30 PM – 5:30 PM

Event Type: Special Session (Research)

Topic Area(s): Autonomous Systems, Cloud

Room: 3001, 3rd Floor

Organizer(s): Dawei Chen, Toyota Motor North America; Ziran Wang, Purdue University

The recent development of cloud computing and edge computing bring forward numerous novel technologies that could play a critical role in realizing the vision of future Connected and Automated Vehicles (CAVs). By enabling CAVs to offload their massive on-board data and heavy computing tasks to road side units (RSUs) at the edge and computing clusters in the cloud, future automotive computing could become more efficient, collaborative, and lower cost. With more communication and sharing via cloud and edge infrastructure, different entities of the future transportation system (e.g., vehicles, road infrastructure, traffic management centers) would become more situation-aware, thus improving the safety, mobility, and environment impact of the entire system. However, to realize this vision, there remain significant challenges to be addressed. This special session will bring four experts from academia and industry to present some of the pressing challenges in cloud- and edge-computing of CAVs and discuss promising directions to address them, including federated learning with multi-access edge computing for CAVs, data management with smart caching at vehicles and wireless network management with dependability constraints, digital twin based design automation tools for development efficiency, and end-to-end methodologies for addressing safety and security in edge-cloud computing of CAVs.

FEDERATED LEARNING AND ANALYSIS WITH MULTI-ACCESS EDGE COMPUTING FOR CONNECTED AND AUTOMATED VEHICLES

Zhu Han, University of Houston, Houston, TX

VEHICLE AS A CACHE – EDGE COMPUTING FOR AUTOMATED DATA CENTRIC VEHICLES

Rolf Ernst, Technische Universität Braunschweig, Germany

AUTONOMOUS DRIVING DIGITAL TWIN EMPOWERED DESIGN AUTOMATION: AN INDUSTRY PERSPECTIVE

Bo Yu, PerceptIn, Shenzhen, China

WAVING THE DOUBLE-EDGED SWORD: BUILDING RESILIENT CAVS WITH EDGE AND CLOUD COMPUTING

Qi Zhu, Northwestern University, Evanston, IL

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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ASK ME ANYTHING WITH RAMKI BALASUBRAMANIAM

Time: 3:30 PM – 4:15 PM

Event Type: Transformative Technologies Theater

Topic Area(s): Cloud

Room: Transformative Technologies Theater, Level 1 Exhibit Hall

Join Ramki Balasubramaniam for an interactive session, where Ramki will answer questions relevant to chip design on cloud.

Cloud has become an indispensable part of EDA/HPC strategy to accelerate Semiconductor workflows and design cycles. Here are some key areas of focus that we deal with in EDA:

1. Cloud workflow migration strategies: as cloud becomes a sustainable component of infrastructure for EDA, taking the effort to migrate workflows to the cloud becomes a key enabler. This has many advantages, as well as challenges. How do we decide on the right priorities?
2. Verification cloud capacity planning: Verification remains the dominant compute demand for EDA. The profile of verification lends itself to flexible strategies. What are some capacity planning considerations that work, and what may be challenging as you navigate the cloud?
3. EDA Data management for optimizing cloud: EDA data comes in many sizes and demand profiles. Using cloud and on-premise data effectively requires good planning.
4. IT strategies for secure cloud: A secure cloud infrastructure is table stakes for cloud service providers today. How do you use this foundation to build an end-to-end secure cloud for your enterprise?
5. Tool characteristics for optimizing cloud: what do you look for in a tool for optimizing your usage in mixed on-premise/cloud environments?
6. AI as a lever: where do you use AI, and how do you decide the value proposition?

Presenter: Ramki Balasubramaniam, AMD, Frisco, TX

TUESDAY ENGINEERING TRACK POSTER PRESENTATIONS

Time: 5:00 PM – 6:00 PM

Event Type: Engineering Track Poster

Room: Level 2 Exhibit Hall

A DESIGN ANALYTICS-BASED METHODOLOGY FOR ENHANCING DYNAMIC IR SIGNOFF WITH MINIMUM DESIGN CHANGES.

Amit Singh, Govind Pal, Sanjeev Jain, Atul Bhargava, STMicroelectronics, Noida, India; Anil Yadav, STMicroelectronics, Gautam Buddha Nagar, India; Amit Jangra, Koshy John, Ansys, Noida, India

A DIGITAL EMULATOR FOR AN ANALOG CONTINUOUS TIME SIGMA DELTA MODULATOR

Ankur Bal, Vikram Singh, STMicroelectronics, Noida, India

A MULTIPHYSICS SIMULATION FLOW FOR HIGH PERFORMANCE MMIC PRODUCTS FOR POWER 5G AND RF APPLICATIONS

Vittorio Cuoco, Ampelon, Nijmegen, Netherlands

A NOVEL FITTING METHOD OF PACKAGE MATERIAL PARAMETERS BASE ON MOP

Xinxin Dong, Feng Wu, Yuan Kai, Jiangtao Zhang, Keqing Ouyang, Sanechips Technology Co., Yongsheng Guo, Ansys, Shanghai, China

A NOVEL METHODOLOGY FOR EM/IR ANALYSIS OF COMPLEX LDO/POWER GATED DESIGNS

Pavan Bilekallu, Debprasad Nandi, Ranjini Gowda, Qualcomm, Bangalore, India

A STATISTICAL APPROACH TO IDENTIFY WASTED POWER CONSUMPTION IN COMBINATIONAL CLUSTERS

Mohammed Fahad, Manish Kumar, Siemens EDA, Noida, India; Mahima Jain, Sachin Kumar, Bhupesh Prajapat, Siemens EDA, Delhi, India; Parul Dohare, Siemens EDA, Varanasi, India

A VERIFICATION PLAN TO ASSESS THE QUALITY OF MOBILE TELEPHONY IN BRAZIL

Joel Oliveira, UFRN, Natal, Brazil

ACCURATE BEHAVIORAL MODELING TECHNIQUE FOR SIMULTANEOUS ACTIVE MULTIPLE LVDS LINE DRIVER

Natish Singla, Saurabh Srivastava, Atul Bhargava, STMicroelectronics, Noida, India; Mihir Pratap, Anil Dwivedi, STMicroelectronics, Delhi, India

ADDRESSING COMMON VERIFICATION PITFALLS OF CHIPLET INTERCONNECTS

Anunay Bajaj, Cadence Design Systems, Inc., Delhi, India; Hemlata Bist, Rohit Mishra, Cadence Design Systems, Inc., Noida, India; Harshit Jaiswal, Cadence Design Systems, Inc., Bangalore, India

AUTO-DETECTION AND UNRAVELING THE REASONS FOR THE UNOPTIMIZED NETS

Balaji Rao Jami, Kishore Kota, Madhu Pappu, Intel, Bangalore, India

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TUESDAY ENGINEERING TRACK POSTER PRESENTATIONS (CONTINUED)

AUTOMATED DESIGN-AWARE OPTIMIZED FILL METHODOLOGY

YoungRye Cho, Ji Young Shin, BonHyuck Koo, Samsung Electronics, Hwaseong, South Korea; SungJin Moon, Siemens EDA, Seoul, South Korea; Yohan Seo, Siemens EDA, Irvine, CA; Dina Medhat, Siemens EDA, Cairo, Egypt

BRIDGING THE GAP BETWEEN NEURAL NETWORK EXPLORATION AND HARDWARE IMPLEMENTATION

Nermine Ali, Michal Szczepanski, Suresh Pajaniradja, Université Paris-Saclay, Paris, France; Ronan Poirier, Siemens EDA, Grenoble, France; Pascal Vivet, Université Grenoble Alpes, Saint-Martin-d'Hères, France

CAMELUS: SCALABLE AND GENERIC SIMD PROGRAMMING FOR AI ACCELERATORS

Xiaofeng Guan, Hao Zhou, Zhengping Hu, Enflame Technology, Beijing, China; Jianguo Yao, Shanghai Jiao Tong University, Shanghai, China

CONSIDERATIONS FOR ACCELERATING AND EFFICIENT USE OF CHIP DESIGN IN THE CLOUD

Taeil KIM, Naya Ha, Sangyun Kim, Samsung Electronics, Hwaseong, South Korea

CORRECT-BY-CONSTRUCT NETLIST BASED INTEGRATION FLOW FOR MIXED-SIGNAL LOW POWER MULTI CHIP MODULE

Lakshmanan Balasubramanian, Penchalkumar Gajula, Avinash Chaudhary, Sumantha Madhyastha, Gaurav Varshney, Texas Instruments (India) Pvt. Ltd., Bangalore, India; Krithika Nanya, KarMic Design Private Limited, Karnataka, India

CREDIT BASED SCHEDULING FOR PRECISION TIME PROTOCOL FRAMES IN AUTOMOTIVE ETHERNET

Vedansh Seth, Cadence Design Systems, Inc., Varanasi, India; Shubham Agarwal, Cadence Design Systems, Inc., San Jose, CA

DERIVING OPTIMAL UNIQUE MULTI INSTANCES IN LARGE SOCS

Srinivasa R STG, Govinda Rajulu STG, Intel, Bangalore, India

DESIGN AND VERIFICATION OF AXI4 MASTER FOR ASIC USING HIGH LEVEL SYNTHESIS IN C++

Dooyoung Go, Moonsoo Kim, Telechips, Gyeonggi-do, South Korea; William Lee, Siemens EDA, Seoul, South Korea

DESIGN FOR TESTABILITY IN ASYNCHRONOUS DIGITAL CONTROLLERS: AN AUTOMATED FLOW TO DESIGN AND VALIDATE ASYNCHRONOUS LOGIC FOR DIGITAL CONTROLLERS

Enea Dimroci, Roberta Priolo, Francesco Battini, Marco Leo, STMicroelectronics, Milano, Italy

EARLY IR DROP PREDICTION USING MACHINE LEARNING FOR POWER GRID

Anil DSouza, Intel, Bangalore, India; Anantha Krishnan A.K, Intel, Kollam, India; Ayan Roy Chowdhury, Intel, Karnataka, India

EFFICIENT WAY OF MIGRATION & COMPARISON OF CUSTOM IC SCHEMATIC DESIGNS

Mahesh Zanwar, Badrinarayan Zanwar, Cadence Design Systems, Inc., Bangalore, India; Stephanie Youssef, Cadence Design Systems, Inc., San Jose, CA; Prashanta Ranabijuli, Cadence Design Systems, Inc., Round Rock, TX

GLOBAL PLACEMENT EXPLOITING STANDARD CELL MERGING CONSTRAINT FOR EFFECTIVE SEMI-CUSTOM DESIGN OPTIMIZATION

Zixiao Wang, Yang Liu, Jing Wang, Qiuling Zeng, HiSilicon, Shenzhen, China; Dmitry Yakimets, Huawei, Leuven, Belgium

HIERARCHICAL POWER GRID ANALYSIS FOR 3D-IC

Kyoungman Han, Yelim Lee, Jaeho Lee, Jiwoo Hong, YoungHoe Cheon, Daehee Lee, Jungyun Choi, Samsung Electronics, Hwaseong, South Korea

IS YOUR STRUCTURAL CDC SIGN-OFF COMPLETE?

Krithivas Krishnaswami, NVIDIA, Hillsboro, OR; Vivek Gupta, NVIDIA, Sunnyvale, CA; Louis Cardillo, NVIDIA, Santa Clara, CA; Varun Sharma, Vikas Sachdeva, Real Intent Inc, Bangalore, India

LAYOUT PROXIMITY EFFECT ON INTERCONNECT CAPACITANCE

Ning Lu, IBM, Poughkeepsie, NY; Richard Wachnik, IBM, Yorktown Heights, NY

LOW POWER DTCO OF FINFET LOGIC PROCESS FOR STACKED CMOS IMAGE SENSOR

Byul Choi, Samsung Electronics, Hwaseong, South Korea

MATHLIB – MATH FUNCTIONS LIBRARY FOR SYSTEMVERILOG/UVM

Srinivasan Venkataramanan, Deepa Palaniappan, VerifWorks, Bangalore, India; Anirudh Srinivasan, King's College London, Palo Alto, CA; Nambi U, Lyle Technologies, Coimbatore, India

PACKET PROCESSING SCALING A FLEXIBLE SCALABLE APPROACH

Pushkar Upadhye, Marvell, Pune, India

PHY VERIFICATION IP

Mrunal Pancholi, Cadence Design Systems, Inc., Gujarat, India; Nehal Patel, Cadence Design Systems, Inc., Gujarat, India

PRE-SILICON POWER SIDE-CHANNEL SECURITY VERIFICATION FOR CRYPTO IPS

Amitabh Das, AMD, Austin, TX; Emrah Karagoz, AMD, Boca Raton, FL; Geethu Babu, Ansys, Burnaby, Canada; Sreeja Chowdhury, Ansys, San Jose, CA

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TUESDAY ENGINEERING TRACK POSTER PRESENTATIONS (CONTINUED)

PREVENTING ITERATIONS FROM SOC IMPLEMENTATION STAGE BY DEVELOPING PIN ACCESSIBLE STANDARD CELL LIBRARY

Sharmistha Sinha, STMicroelectronics, Bangalore, India; Anand Mishra, Anuradha Ray, Atul Bhargava, STMicroelectronics, Greater Noida, India; Frederic Avellaneda, STMicroelectronics, Lyon, France; Parul Agrawal, Cadence Design Systems, Inc., Agra, India; Hitesh Marwah, Cadence Design Systems, Inc., Noida, India; Neha Agrawal, Cadence Design Systems, Inc., San Jose, CA; Vishesh Kumar, Cadence Design Systems, Inc., Bangalore, India

RETHINKING THE USAGE OF SELF-CONTAINED REUSABLE COMPONENTS

Ali El-Zein, Maya Safieddine, Viresh Paruthi, IBM, Austin, TX; Stephen Barnfield, IBM, San Jose, CA

RF SIMULATION METHODOLOGY IN S-PARAMETER & PERIODIC STEADY STATE & PHASE NOISE ANALYSIS

Kihoon Kim, SK Ryu, Seongkyun Shin, Samsung Electronics, Hwaseong, South Korea

SCHEMATIC AWARE IP COMPILER: IMPROVING PRODUCTIVITY WITH RELATIVE PLACEMENT

Bhupendra Vishwakarma, Cadence Design Systems, Inc., Bangalore, India

SILICON DEBUG OF REAL TIME CLOCK MACRO USING NANOPROBING TECHNIQUE

Krishnan Sukumar, Ravindra Ayyagari, Animesh Jain, Santosh Vodnala, AMD, Bangalore, India; Soon-Huat Lim, AMD, Singapore, Singapore

SOLVING THE RANDOMIZATION CHALLENGE IN CPU VERIFICATION

Karthik Rajakumar, Pooja Madhusoodhanan, Texas Instruments, Bangalore, India

SPICE VALIDATION OF DYNAMIC VOLTAGE DROPS FROM SIGMADVD

Andy Hoover, Samsung Electronics, Austin, TX; Kevin Klein, Samsung Electronics, Hwaseong, South Korea; Ed Deeters, Jeff Linn, Ansys, Austin, TX

STATISTICAL IR ANALYSIS WITH ANSYS SIGMADVD

Pranav Ranganathan, Microsoft, Raleigh, NC; Chip Stratakos, Microsoft, Saratog, CA; Medha Kulkarni, Microsoft, Mountain View, CA

UNIFIED SOLUTION FOR CAD DEVELOPMENT OF ANALOG, DIGITAL & MIXED SIGNAL IPS

Lippika Parwani, Bhupendra Singh, Gaurav Goel, STMicroelectronics, Noida, India; Anil-kumar Dwivedi, STMicroelectronics, Delhi, India

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WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 PM – 7:00 PM

Event Type: Work-in-Progress Poster

Room: Level 2 Lobby

A CNN-BASED CODE ASSISTANCE FOR LAYOUT-TO-GENERATOR CONVERSION OF ANALOG CIRCUITS

Sungyu Jeong, Minsu Kim, Byungsub Kim, Pohang University of Science and Technology, Pohang, South Korea

A COMPUTATION INTERLEAVING COUNTERMEASURE AGAINST PROFILED SIDE CHANNEL ATTACKS

Isabella Piacentini, Alessandro Barenghi, Gerardo Pelosi, Politecnico di Milano, Milan, Italy

A COST-GENERIC LOGIC SYNTHESIS FRAMEWORK WITH CUSTOMIZABLE COST FUNCTIONS

Hanyu Wang, ETH Zürich, Zurich, Switzerland; Siang-Yun Lee, Giovanni De Micheli, École Polytechnique Fédérale de Lausanne, Switzerland

A DISCRETE 2.5D CHIPLET LIBRARY AND OPTIMIZED MAPPING OF AI ALGORITHMS FOR HETEROGENEOUS IN-MEMORY ACCELERATION

Zhenyu Wang, Gopikrishnan Raveendran Nair, Gokul Krishnan, Jaesun Seo, Chaitali Chakrabarti, Yu Cao, Arizona State University, Tempe, AZ; A. Alper Goksoy, Umit Ogras, University of Wisconsin, Madison, WI

A NOVEL SENSOR FUSION TECHNIQUE FOR 2D OBJECT DETECTION FOR SELF-DRIVING CARS

Jisup Lee, YoungJin Kim, Soonhoi Ha, Seoul National University, Seoul, South Korea

A NOVEL TECHNIQUE TO SUPPORT DEEP LEARNING APPLICATIONS IN A MODEL-BASED EMBEDDED SOFTWARE DESIGN METHODOLOGY

Jangryul Kim, Jaewoo Son, Soonhoi Ha, Seoul National University, Seoul, South Korea

A PROCESSING ELEMENT FOR SPARSE TENSOR ACCELERATORS

Midia Reshadi, David Gregg, Lero, Trinity College, Dublin, Ireland

A STAND-ALONE VIRTUAL PLATFORM RUNNABLE AT UNIFIED TIME DOMAIN AS NVME SSD FULL-SYSTEM SIMULATOR

Beomchan Park, Jeehoon Choi, Byunghoon Lee, Jongseong Park, Kyoungbum Kim, Samsung Electronics, Hwaseong, South Korea

ABC-DE : ABC DESIGN EXPLORER FOR LUT-BASED SYNTHESIS

Thierry Besson, Pierre-Emmanuel Gaillardon, Rapid Silicon, Los Gatos, CA

ACCELERATING EXACT COMBINATORIAL OPTIMIZATION VIA RL-BASED INITIALIZATION – A CASE STUDY IN SCHEDULING

Jiaqi Yin, Cunxi Yu, University of Utah, Salt Lake City, UT

AMACC: ASYNCHRONOUS MEMORY ACCESS ACCELERATOR FOR RISC-V EMBEDDED SOFT PROCESSORS

Songyue Wang, Luming Wang, Tianyue Lu, Mingyu Chen, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

AN EFFICIENT SPLIT FINE-TUNING FRAMEWORK FOR EDGE AND CLOUD COLLABORATIVE LEARNING

Shaohuai Shi, Shuhan Qi, Xuan Wang, Harbin Institute of Technology, Shenzhen, China; Qing Yang, Yang Xiang, Peng Cheng Laboratory, Shenzhen, China

AN ML BASED SEMI-STATIC PREDICTOR FOR APPROXIMATE LOAD VALUE IN CACHE MEMORY

Alain Aoun, Concordia University, Montreal, Canada; Mahmoud Masadeh, Yarmouk University, Irbid, Jordan; Sofiene Tahar, Concordia University, Montreal, Canada

ANALOG SYSTEM HIGH-LEVEL SYNTHESIS TO PHYSICAL DEVICES

Afolabi Ige, Linhao Yang, Hang Yang, Cong “Callie” Hao, Jennifer Halser, Georgia Institute of Technology, Atlanta, GA

AUTOSPARE: AUTOMATIC SEARCH FOR EFFICIENT ACTIVATION SPARSITY-AWARE CNN ACCELERATOR

Sumin Kim, Taeyun An, Youngmin Yi, University of Seoul, Seoul, South Korea

COUNTERING THE PATH EXPLOSION PROBLEM IN THE SYMBOLIC EXECUTION OF HARDWARE DESIGNS

Kaki Ryan, Cynthia Sturton, University of North Carolina, Chapel Hill, NC

CRAN: A COMPUTATIONAL REDUNDANCY-AWARE ACCELERATOR FOR CONVOLUTIONAL NEURAL NETWORKS

Yongjun Kim, Seongwook Kim, Yujin Kim, Gwangeun Byeon, Prashant Jayaprakash, Seokin Hong, Sungkyunkwan University, Suwon, South Korea

CTSCAN: A CGRA-BASED PLATFORM FOR EMULATION OF POWER SIDE-CHANNEL ATTACKS ON CPUS

Yaswanth Tavva, Rohan Juneja, Trevor E. Carlson, Li-Shiuan Peh, National University of Singapore, Singapore

CUKNIT: OPTIMIZED PARTITIONING OF QUANTUM CIRCUITS USING KNITTING AND CUTTING

Sebastian Brandhofer, Iliia Polian, University of Stuttgart, Germany; Kevin Krsulich, IBM, Yorktown Heights, NY

DEEPSEQ: DEEP SEQUENTIAL CIRCUIT LEARNING

Sadaf Khan, Zhengyuan Shi, Min Li, Qiang Xu, The Chinese University of Hong Kong, Hong Kong

DESIGN SPACE EXPLORATION OF LAYER-WISE MIXED-PRECISION QUANTIZATION WITH TIGHTLY INTEGRATED EDGE INFERENCE UNITS

Xiaotian Zhao, Ruge Xu, Xinfei Guo, Shanghai Jiao Tong University, Shanghai, China; Yimin Gao, Vaibhav Verma, Mircea Stan, University of Virginia, Charlottesville, VA

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WORK-IN-PROGRESS POSTER SESSION (CONTINUED)

DYBIT: DYNAMIC BIT-PRECISION NUMBERS FOR EFFICIENT QUANTIZED NEURAL NETWORK INFERENCE

Jiajun Zhou, Jiajun Wu, Yizhao Gao, Yuhao Ding, Chaofan Tao, Boyu Li, Hayden So, Ngai Wong, The University of Hong Kong, Hong Kong; Fengbin Tu, Tim Cheng, Hong Kong University of Science and Technology, Hong Kong

EFFICIENT ACCELERATOR INTEGRATION WITH GENERATED MODULES

Tuo Dai, Bizhao Shi, Guojie Luo, Peking University, Beijing, China

EFFICIENT PARETO POINT PROPAGATION ALGORITHM FOR HLS DESIGN SPACE EXPLORATION

Chang Wu, Fudan University, Shanghai, China; Wenqing Wan, Shanghai Fudan Microelectronics Group Co., Ltd., Shanghai, China

ENABLING EFFICIENT NVM-BASED TEXT ANALYTICS WITHOUT DECOMPRESSION

Xiaokun Fang, Feng Zhang, Junxiang Nong, Puyun Hu, Yunpeng Chai, Xiaoyong Du, Renmin University of China, Beijing, China; Mingxing ZHANG, Tsinghua University, Beijing, China

EPIM: EFFICIENT PROCESSING-IN MEMORY ACCELERATORS BASED ON EPITOME

Chenyu Wang, Zhenhua Zhu, Tsinghua University, Beijing, China; Zhen Dong, Kurt Keutzer, University of California, Berkeley, CA; Daquan Zhou, Bytedance, Singapore, Singapore; Jiashi Feng, National University of Singapore, Singapore

FEEDBACK BUFFER INSERTION: AN EFFICIENT METHOD FOR PIPELINED PROCESSORS DESIGN WITH HIGH-LEVEL SYNTHESIS

Yuhan She, Jierui Liu, Yanlong Huang, Weipei Huang, Ray Cheung, Hong Yan, City University of Hong Kong

FLEXNAS: FLEXIBLE HARDWARE AWARE TRAINING-LESS NEURAL ARCHITECTURE SEARCH FOR FPGAS

Chengdi Cao, Lorenzo Ferretti, Suhail Basalama, Jason Cong, University of California, Los Angeles, CA

FSMGEN: BRIDGING HIGH-LEVEL SPECIFICATION AND LOW-LEVEL HARDWARE CONSTRUCTION ON FPGAS

Zizhang Luo, Youwei Xiao, Yun (Eric) Liang, Peking University, Beijing, China

FUNTOM: FUNCTIONAL MODELING OF RF CIRCUITS USING A NEURAL NETWORK ASSISTED TWO-PORT ANALYSIS METHOD

Morteza Fayazi, Morteza Tavakoli Taba, Amirata Tabatabavakili, Ehsan Afshari, University of Michigan, Ann Arbor, MI; Ronald Dreslinski, Un

FUZZING AND STATIC ANALYSIS GUIDED SYMBOLIC EXECUTION TO DETECT HARDWARE TROJANS

Ruo Chen Dai, Tuba Yavuz, University of Florida, Gainesville, FL

GPP-MAP: GRAPH NEURAL NETWORK AND POLYHEDRAL MODEL ASSISTED PARALLEL CGRA MAPPING OPTIMIZATION FRAMEWORK

Bizhao Shi, Tuo Dai, Jiayi Zhang, Xuechao Wei, Guojie Luo, Peking University, Beijing, China; Hongzhong Zheng, Alibaba Group, Sunnyvale, CA; Yuan Xie, University of California, Santa Barbara, CA

GRAPH MACHINE LEARNING ASSISTED ANALOG CIRCUIT DESIGNING

Aditya Shahane, Saripilli Swapna Manjiri, Sandeep Kumar, Ankesh Jain, Indian Institute of Technology, Delhi, India

HOW CONNECTION DELAY CAN AFFECT SYNCHRONIZATION WITH TWO-FACTOR TOOLS

Joel Goncalves Oliveira, Sao Jose do Campestre, Brazil; Márcio Kreutz, UFRN, Natal, Brazil

HUGFUZZ: HUMAN-GUIDED FUZZING FOR RTL DESIGNS

Yuichi Sugiyama, Reoma Matsuo, Ryota Shioya, The University of Tokyo, Japan

IAM: A PROTOCOL TO IMPROVE SECURITY IN ISO 15118-20 EV CHARGING VIA REMOTE ATTESTATION

Ross Porter, Morteza Biglari-Abhari, Duleepa Thrimawithana, University of Auckland, Auckland, New Zealand; Benjamin Tan, University of Calgary, Canada

IMPROVING BLOCK MANAGEMENT IN 3D NAND FLASH MEMORY USING SUB-BLOCK FIRST PAGE WRITE SEQUENCE

Matchima Buddhano, Aleksandar Milenkovic, Biswajit Ray, University of Alabama, Huntsville, AL

INTERLEAVING-MAPPING: A NOVEL DATA LAYOUT IN SPRAM

Zhang Dunbo, Zeng Lingling, Lang Qingjie, Xun Changqing, Shen Li, National University of Defense Technology, Changsha, China

LAYNET: LAYOUT SIZE PREDICTION FOR MEMORY DESIGN USING GRAPH NEURAL NETWORKS IN EARLY DESIGN STAGE

Hye Rim Ji, Jong Seong Kim, Jung Yun Choi, Samsung Electronics, Hwaseong, South Korea; Jee Hyong Lee, Sungkyunkwan University, Suwon, South Korea

LIGHTFUSION: LIGHTWEIGHT CNN ARCHITECTURE FOR ENABLING EFFICIENT SENSOR FUSION IN AUTONOMOUS DRIVING

Qingliang Liu, Shuai Zhou, Jinmei Lai, Fudan University, Shanghai, China

LUNAR: A NATIVE TABLE ENGINE FOR IOT DEVICES

Xiaopeng Fan, Song Yan, Chuliang Weng, East China Normal University, Shanghai, China

MACHINE-LEARNING BASED NETLIST REDUCTION FOR EFFICIENT VARIATION-AWARE DELAY CHARACTERIZATION IN SRAM

Inseong Jeon, Hyunho Park, Junseo Lee, Taehwan Yoon, Hanwool Jeong, Kwangwoon University, Seoul, South Korea

Research Sessions

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WORK-IN-PROGRESS POSTER SESSION (CONTINUED)

MCUGEN: MEMORY EFFICIENT MAPPING AND CODE GENERATION FOR DNN INFERENCE ON MCUS

Size Zheng, Renze Chen, Meng Li, Runsheng Wang, Ru Huang, Yun (Eric) Liang, Peking University, Beijing, China

MINING SOC MESSAGE FLOWS WITH SELF-ATTENTION

Md Rubel Ahmed, University of South Florida, Tampa, FL; Bardia Nadimi, University of South Florida, Tampa, FL; Hao Zheng, University of South Florida, Tampa, FL

NEUROMORPHIC SYSTEM-ON-CHIP TOWARDS EFFICIENT EDGE HEALTHCARE

Fengshi Tian, Jingyu He, Xiaomeng Wang, Jia Chen, Fengbin Tu, Chi Ying Tsui, Tim Cheng, Hong Kong University of Science and Technology, Hong Kong; Jinbo Chen, Shiqi Zhao, Jie Yang, Mohamed Sawan, Westlake University, Hangzhou, China

NODE-LEVEL DYNAMIC DISTRIBUTED TRUST METRIC EVALUATION

Rakibul Hassan, Sai Manoj Pudukotai Dinakarrao, George Mason University, Fairfax, VA

OPTIMAL ANN-TO-SNN CONVERSION FRAMEWORK FOR LSTMS

Gourav Datta, Haoqin Deng, Robert Aviles, Zeyu Liu, Peter, Beerel, University of Southern California, Los Angeles

QUADRANET: IMPROVING HIGH-ORDER NEURAL INTERACTION EFFICIENCY WITH HARDWARE-AWARE QUADRATIC NEURAL NETWORKS

Chenhui Xu, George Mason University, Fairfax, VA; Fuxun Yu, George Mason University, Fairfax, VA; Zirui Xu, George Mason University, Fairfax, VA; Chenchen Liu, University of Maryland, Baltimore County, Baltimore, MD; Jinjun Xiong, University at Buffalo, B

QUBIT MAPPING TOWARD QUANTUM ADVANTAGE

Chien-Yi Yang, University of California, San Diego, CA; RenChu Wang, Georgia Institute of Technology, Atlanta, GA; Chin-Yi Cheng, Yi-Hsiang Kuo, Hao-Chung Cheng, Chung-Yang Huang, National Taiwan University, Taipei, Taiwan

QUICKLOOP: AN EFFICIENT, FPGA-ACCELERATED EXPLORATION OF PARAMETERIZED RTL GENERATORS

Tayyeb Mahmood, Jaeyong Chung, Incheon National University, Incheon, South Korea

REAL-TIME DEEP VISUAL TRACKING ON A TIGHT BUDGET

Minh Do Van, Meiqing Wu, Siew-Kei Lam, Thambipillai Srikanthan, Nanyang Technological University, Singapore

RECONFIGURABLE NETWORK-ON-CHIP ARCHITECTURE FOR INTRA-CLUSTER COMMUNICATION ON SPIKING NEUROMORPHIC HARDWARE

Manu Rathore, Adam Foshie, Garrett Rose, University of Tennessee, Knoxville, TN

RECTIFICATION LEARNING FROM HYPOTHESES REFUTATION AND RELEVANCE CLASSIFICATION

Victor Kravets, IBM, New York, NY; Jie-Hong Roland Jiang, National Taiwan University, Taipei, Taiwan; Gi-Joon Nam, IBM Research, Yorktown Heights, NY

RODOS: ROBUST DESIGN OPTIMIZATION WITH SIMULATOR LEARNING

Youngmin Oh, Doyun Kim, Bosun Hwang, Samsung Electronics, Hwaseong, South Korea

SEASONS: SIGNAL AND ENERGY AWARE SENSING ON INTERMITTENT SYSTEMS

Pouya Mahdi Gholami, Henry Hoffmann, University of Chicago, IL

SECGRAPH: SECURITY ORIENTED GRAPH NEURAL NETWORK ASSISTED PROTECTION ON HARDWARE

Weimin Fu, Xiaolong Guo, Kansas State University, Manhattan, KS; Yier Jin, University of Florida, Gainesville, FL; Kaichen Yang, Michigan Technological University, Houghton, MI

SECURE RUN-TIME HARDWARE TROJAN DETECTION USING LIGHTWEIGHT ANALYTICAL MODELS

Burin Amornpaisannon, Andreas Diavastos, Li-Shiuan Peh, Trevor E. Carlson, National University of Singapore, Singapore

SECURITY: A DESIGN APPROACH FOR ENHANCING SOC SECURITY

Naorin Hossain, Margaret Martonosi, Princeton University, Princeton, NJ; Alper Buyuktosunoglu, John-David Wellman, Pradip Bose, IBM, Yorktown Heights, NY

SUPERFLOW: A RTL-TO-GDS DESIGN FLOW FOR AQFP SUPERCONDUCTING DEVICES

Yanyue Xie, Peiyan Dong, Geng Yuan, Zhengang Li, Chao Wu, Sung-En Chan, Xufeng Zhang, Yanzhi Wang, Northeastern University, Boston, MA; Olivia Chen, Tokyo City University, Tokyo, Japan; Nobuyuki Yoshikawa, Yokohama National University, Yokohama, Japan

TETRIS-SDK: EFFICIENT CONVOLUTION LAYER MAPPING WITH ADAPTIVE WINDOWS FOR FAST IN MEMORY COMPUTING

Ke Dong, Bo Wang, Singapore University of Technology and Design, Singapore, Singapore; Kejie Huang, Zhejiang University, Hangzhou, China

TOWARDS LARGE-SCALE ROUTING: A NOVEL LEARNING BASED DIVIDE & MERGE APPROACH

Liyang Yang, Guowei Sun, Hu Ding, University of Science and Technology of China, Hefei, China; Lin Chen, Anhui University, Hefei, China

WEAR LEVELING OF PROCESSING ELEMENTS ARRAY IN DEEP NEURAL NETWORK ACCELERATORS

Taesoo Lim, Hyeonjin Kim, Jingu Park, Bogil Kim, William Song, Yonsei University, Seoul, South Korea

WA-PUF: WRITE-ASSIST AUGMENTATION OF SEQUENCE DEPENDENT SRAM PUF FOR ENHANCED RANDOMNESS AND UNIQUENESS

Kailash Prasad, Alok Pradhan, Joycee Mekie, Indian Institute of Technology, Gandhinagar, India

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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PROGRAM

Wednesday, July 12, 2023

WEDNESDAY KEYNOTE: WALDEN RHINES AND VISIONARY TALK: LIP-BU TAN

Time: 8:40 AM – 10:00 AM

Event Type: Keynote, Visionary Talk

Topic Area(s):

Room: 3020, 3rd Floor

INTRODUCTION AND AWARDS

ADVANCING PRECISION MEDICINE THROUGH GENERATIVE AI-DRIVEN DRUG DEVELOPMENT

Lip-Bu Tan, Walden International

TAKING AI TO THE NEXT LEVEL

Walden Rhines, Cornami, Inc., Dallas, TX

THE AI HARDWARE SHOW LIVE: SILICON OR SURVIVAL

Time: 10:15 AM – 11:15 AM

Event Type: Analyst Presentation

Topic Area(s): AI

Room: DAC Pavilion, Level 2 Exhibit Hall

In this session, The AI Hardware Show goes on the road. Co-hosts Sally and Ian will walk through the landscape of currently available and upcoming AI Hardware focused for the DAC audience. This presentation will start with a wide overview of the types of architectures currently in play with hardware solutions, from CPU to GPU to ASIC to optical and neuromorphic and others, as well as the different logical architectures being used. The second half of the presentation covers the AI Hardware market from the chip and IP perspective, both for the main established players as well as the current state of funding for AI Hardware startups. In this latter segment, present and future hardware solutions will be discussed as well as their applicability to training, inference, and where noted, design workloads.

Presenters: Ian Cutress, More Than Moore, London, United Kingdom; Sally Ward-Foxton, EE-Times, London, United Kingdom

HARDWARE AND SOFTWARE TECHNOLOGIES CONTINUE TO ADVANCE, IN CLOSE COLLABORATION

Time: 10:30 AM – 12:00 PM

Event Type: Engineering Tracks

Topic Area(s): Back-End Design

Room: 2008, Level 2

Organizer: Sabya Das, Synopsys, Mountain View, CA

To continue the advancement of the semiconductor, hardware and software technologists need to work and innovate together. This session focuses on the progress in that that collaborative research space. The first talk describes a notional system architecture and a cross-cutting approach connecting innovations in compute algorithm, chip architecture, and system software. The second talk is about finding post-Silicon issues in the pre-silicon validation phase that will shorten the software bring-up time on Silicon. The speaker will talk about first deconstructing the problem in the user domain and then constructing the solution in the EDA domain. Focus of the third talk is on a new agile methodology for co-designing programmable hardware accelerators and compilers. This methodology employs a combination of new programming languages and formal methods to automatically generate the accelerator hardware and its compiler from a single source of truth.

Moderator: Bertram Bradley, Marvell, Austin, TX

Panelists: Saibal Mukhopadhyay, Georgia Institute of Technology, Atlanta, GA; Ribhu Mittal, Synopsys, Hillsboro, OR; Priyanka Raina, Stanford University, Stanford, CA

VERIFICATION BEYOND COVERAGE

Time: 10:30 AM – 12:00 PM

Event Type: Engineering Tracks

Topic Area(s): Front-End Design

Room: 2010, 2nd Floor

Organizer(s): Hari Mony, Synopsys, Austin, TX

Session Chair: Ram Narayan, ARM

Verification processes use coverage metrics to take rather significant decisions, but coverage is not what it used to be. While coverage metric slowly changed focus towards test plan/testbench coverage, the needs of verification also changed, from hunting the exceedingly unlikely bug to making sure given application(s) (SW) run without a hitch. The most important innovation brought by functional coverage was to increase observability of the DUT during simulation, but coverage now can easily delude our demands, sometimes because of the lack of awareness but mostly because coverage might not be the right means to capture them. Coverage is here to stay, but did our verification demands outgrow “coverage”? What would the “beyond coverage” life be?

Presenters: Adnan Hamid, Breker, San Jose, CA; Mark Glasser, Elastics Systems, Soquel, CA; Matt Graham, Cadence Design Systems, Inc., Cork, Canada; David Lacey, Hewlett Packard Enterprise, Palo Alto, CA

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Engineering Track

DELIVERING ON RISC V'S PROMISE TO GIVE DESIGNERS FREEDOM TO INNOVATE – WHAT'S NEEDED?

Time: 10:30 AM – 12:00 PM
Event Type: Engineering Tracks
Topic Area(s): IP
Room: 2012, 2nd Floor

Organizer: Larry Lapides, Imperas, Dublin, CA

The RISC-V instruction set architecture (ISA) open standard has accelerating momentum in the semiconductor community. This is due to the open nature of the ISA, enabling users to build domain specific processors that can help to differentiate products. Is this momentum built on real SoCs going to production? What is needed to develop a RISC-V based SoC? How mature is the specification? Is RISC-V ready for prime time?

This panel, from various areas in the RISC-V community / ecosystem from fab through to end user, will try to address these questions and more, and provide their perspectives on the readiness of RISC-V, and the path to RISC-V based silicon.

Moderator: Calista Redmond, RISC-V International, Washington, DC

Panelists: Bob Brennan, Intel, Santa Clara, CA; Rick O'Connor, OpenHW Group, Ottawa, Canada; Simon Davidmann, Imperas, Thame, United Kingdom; Richard Barry, Amazon, Seattle, WA; Himanshu Sanghavi, Meta, Fremont, CA

FANTASTIC AI SYSTEM IMPROVEMENTS AND WHERE TO FIND THEM

Time: 10:30 AM – 12:00 PM
Event Type: Research Manuscript
Topic Area(s): AI/ML System and Platform Design
Room: 3012, 3rd Floor

Session Chair(s): Lingchuan Meng, Amazon; Jinho Lee, Seoul National University

We all agree that AI efficiency improvements are important and the keys to unlock more use cases. But the question is where to find them in the system. This session presents paper that improves inference efficiency by optimizing different parts of an AI system, ranging from non-volatile storage, memory usage, compute instruction packing, and to power management.

LIGHTNING TALK – EMERGING DEVICE TECHNOLOGIES AND SYSTEM INTEGRATION TOWARDS UBIQUITOUS MACHINE INTELLIGENCE

Haitong Li, Purdue University, West Lafayette, IN

INTERMITTENT-AWARE NEURAL NETWORK PRUNING

Chih-Chia Lin, Tei-Wei Kuo, National Taiwan University, Taipei, Taiwan;
Chia-Yin Liu, Chih-Hsuan Yen, Pi-Cheng Hsiu, Academia Sinica, Taipei, Taiwan

OCCAMY: MEMORY-EFFICIENT GPU COMPILER FOR DNN INFERENCE

Jaeho Lee, Shinnung Jeong, Seungbin Song, Kunwoo Kim, Heelim Choi, Youngsok Kim, Hanjun Kim, Yonsei University, Seoul, South Korea

UINT-PACKING: A UNSIGNED FULL-INTEGGER DSP PACKING METHOD MULTIPLES YOUR DNN ACCELERATOR PERFORMANCE

Jingwei Zhang, Meng Zhang, Xinye Cao, Guoqing Li, Southeast University, Nanjing, China

CONDENSE: A FRAMEWORK FOR DEVICE AND FREQUENCY ADAPTIVE NEURAL NETWORK MODELS ON THE EDGE

Yifan Gong, Pu Zhao, Zheng Zhan, Yushu Wu, Chao Wu, Zhenglun Kong, Minghai Qin, Caiwen Ding, Yanzhi Wang, Northeastern University, Boston, MA

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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GREETINGS FROM HARDWARE-FRIENDLY AI ALGORITHMS

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Algorithms

Room: 3004, 3rd Floor

Session Chair(s): Ganapathy Parthasarathy, Synopsys; Xueqing Li, Tsinghua University

AI algorithms have achieved amazing success owing to the complex and expensive computations. Efficient AI has become an important research topic in order to promote the widespread use of AI on various hardware platforms. This session advances the state-of-the-art in this domain by exploring hardware-friendly algorithm optimizations for various AI models. The first two papers discuss the efficient CNN designs, followed by two papers covering the optimizations for Transformers and graph neural networks.

LIGHTNING TALK – HARDWARE-AWARE AI ALGORITHMS TO IMPROVE RESOURCE EFFICIENCY

Jana Doppa, Washington State University, Pullman, WA

NETBOOSTER: EMPOWERING TINY DEEP LEARNING BY STANDING ON THE SHOULDERS OF DEEP GIANTS

Zhongzhi Yu, Yonggan Fu, Haoran You, Yingyan (Celine) Lin, Georgia Institute of Technology, Atlanta, GA; Jiayi Yuan, Rice University, Houston, TX

WINOTRAIN: WINOGRAD-AWARE TRAINING FOR ACCURATE FULL 8-BIT CONVOLUTION ACCELERATION

Pierpaolo Mori, Claudio Passerone, Politecnico di Torino, Turin, Italy; Shambhavi Balamuthu Sampath, Lukas Frickenstein, Manoj Rohit Vemparala, Nael Fafous, Alexander Frickenstein, BMW, Munich, Germany; Walter Stechele, Technische Universität München, Germany

RANGE-INVARIANT APPROXIMATION OF NON-LINEAR OPERATIONS FOR EFFICIENTLY FINE-TUNING BERT

Janghyeon Kim, Janghwan Lee, Jungwook Choi, Hanyang University, Seoul, South Korea; JeongHo Han, Sangheon Lee, SAPEON Korea Inc., Seongnam-si, South Korea

HARDWARE-AWARE GRAPH NEURAL NETWORK AUTOMATED DESIGN FOR EDGE COMPUTING PLATFORMS

Ao Zhou, Jianlei Yang, Yingjie Qi, Yumeng Shi, Tong Qiao, Weisheng Zhao, Chunming Hu, Beihang University, Beijing, China

LEADING DEVELOPMENTS FROM THE FRONTIER OF HIGH-LEVEL SYNTHESIS AND NEIGHBORHOODS

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): RTL/Logic Level and High-level Synthesis

Room: 3002, 3rd Floor

Session Chair(s): Luca Amaru, Synopsys; Jody Matos, Silvaco

New tools for dataflow, datapath and hardware accelerators: architectural optimization and design space exploration by Rubick to synthesize spatial architectures via dataflow decomposition, an FPGA mapping-aware timing regulation technique for dataflow circuits, floating-point hardware optimization by program analysis and equivalence graph rewriting techniques, and finally hardware generation and scheduling for heterogeneous neural network accelerators based on processing-in-memory.

LIGHTNING TALK – THE NEXT WAVE OF HIGH-LEVEL SYNTHESIS

Deming Chen, University of Illinois at Urbana-Champaign, IL

RUBICK: A SYNTHESIS FRAMEWORK FOR SPATIAL ARCHITECTURES VIA DATAFLOW DECOMPOSITION

Zizhang Luo, Size Zheng, Yun (Eric) Liang, Peking University, Beijing, China; Liqiang Lu, Jianwei Yin, Zhejiang University, Hangzhou, China; Jieming Yin, Nanjing University of Posts and Telecommunications, Nanjing, China; Jason Cong, University of California, Los Angeles, CA

AN ITERATIVE METHOD FOR MAPPING-AWARE FREQUENCY REGULATION IN DATAFLOW CIRCUITS

Carmine Rizzi, Lana Josipovic, ETH Zürich, Switzerland; Andrea Guerrieri, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland

AUTOMATING CONSTRAINT-AWARE DATAPATH OPTIMIZATION USING E-GRAPHS

Samuel Coward, Intel, London, United Kingdom; George Constantinides, Imperial College London, United Kingdom; Theo Drane, Intel, Folsom, CA

PIM-HLS: AUTOMATIC HARDWARE GENERATION AND SCHEDULING FOR PROCESSING-IN-MEMORY-BASED NEURAL NETWORK ACCELERATORS

Yu Zhu, Zhenhua Zhu, Hanbo Sun, Huazhong Yang, Yu Wang, Tsinghua University, Beijing, China; Guohao Dai, Shanghai Jiao Tong University, Shanghai, China; Fengbin Tu, Tim Cheng, Hong Kong University of Science and Technology, Hong Kong

Research Sessions

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LET'S NETWORK WITH CHIPLETS

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): Design Methodologies for System-on-Chip and 3D/2.5D System-in Package

Room: 3008, 3rd Floor

Session Chair(s): Sanghamitra Roy, Utah State University; Prabal Basu, Cadence Design Systems, Inc.

The advent of chiplet-based SoC has revolutionized the electronics industry by enabling higher performance and increased scalability. Chiplet-based SoCs consist of multiple smaller chips, called chiplets, which are combined to form a complete system. NoC is an essential component of chiplet-based SoCs, providing high-speed communication between the chiplets and ensuring efficient data transfer. This session presents latest innovations in the realm of chiplet-based system architecture and energy-efficient NoC design. The topics covered range from the benefit of employing chiplets over monolithic design, high-performance chiplet arrangement schema, to customizable traditional NoC design, and ultra-fast optical interconnect topologies.

LIGHTNING TALK – HIGH FIDELITY BENCHMARKING OF INTERPOSER MATERIAL CHOICES USING 2.5D DESIGN TOOLS

Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA

SPARSE HAMMING GRAPH: A CUSTOMIZABLE NETWORK-ON-CHIP TOPOLOGY

Patrick Iff, Maciej Besta, Matheus Cavalcante, Tim Fischer, Torsten Hoefler, ETH Zürich, Zurich, Switzerland; Luca Benini, University of Bologna, Italy

CHIPLETS: HOW SMALL IS TOO SMALL?

Alexander Graening, **Saptadeep Pal**, Puneet Gupta, University of California, Los Angeles, CA

TOWARD PARALLELISM-OPTIMAL TOPOLOGY GENERATION FOR WAVELENGTH-ROUTED OPTICAL NOC DESIGNS

Kuan-Cheng Chen, Yan-Lin Chen, Yu-Sheng Lu, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

HEXAMESH: SCALING TO HUNDREDS OF CHIPLETS WITH AN OPTIMIZED CHIPLER ARRANGEMENT

Patrick Iff, Maciej Besta, Matheus Cavalcante, Tim Fischer, Torsten Hoefler, ETH Zürich, Switzerland; Luca Benini, University of Bologna, Italy

PRACTICAL EDGEAI INFRASTRUCTURE AND APPLICATIONS: EFFICIENCY AND RESILIENCE IN THE WILD

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Application and Infrastructure

Room: 3003, 3rd Floor

Session Chair(s): Cong (Callie) Hao, Georgia Institute of Technology; Ankita Nayak, Stanford University

This session presents four papers that look at the practical design aspects as well as applications of EdgeAI. To tackle the tremendous amount of data generated, the first paper presents a hardware-friendly neural autoregressive framework to improve lossless compression performance. The second paper formulates the microarchitecture design space exploration as Bayesian optimization, and captures the parameter dependencies using graph representation learning. The third paper addresses the burdensome chip HW design requirements extraction task and uses ML to translate timing-diagram images into a symbolic formal specification. The fourth paper proposes enhancing hardware malware detectors (HMD) by leveraging approximate computing techniques to achieve adversarial resiliency.

LIGHTNING TALK – TRENDS AND CHALLENGES IN AI FOR DESIGN: PREDICTION, OPTIMIZATION AND REASONING

Rajeev Jain, University of California, Qualcomm, Los Angeles, CA

FASTER AND STRONGER LOSSLESS COMPRESSION WITH OPTIMIZED AUTOREGRESSIVE FRAMEWORK

Yu Mao, Jingzong Li, Chun Xue, City University of Hong Kong, Hong Kong; Yufei Cui, McGill University, Montreal, Canada

GRAPH REPRESENTATION LEARNING FOR MICROARCHITECTURE DESIGN SPACE EXPLORATION

Xiaoling Yi, Jialin Lu, Li Shang, Fan Yang, Fudan University, Shanghai, China; Xiankui Xiong, Dong Xu, ZTE Corporation, Shanghai, China

TD-MAGIC: FROM PICTURES OF TIMING DIAGRAMS TO FORMAL SPECIFICATIONS

Jie He, Radu Grosu, Vienna University of Technology, Vienna, Austria; Dejan Nickovic, Austrian Institute of Technology, Vienna, Austria; Ezio Bartocci, Technische Universität Wien, Vienna, Austria

STOCHASTIC-HMDS: ADVERSARIAL-RESILIENT HARDWARE MALWARE DETECTORS VIA UNDERVOLTING

Md Shohidul Islam, Khaled N. Khasawneh, George Mason University, Fairfax, VA; Ihsen Alouani, Queen's University Belfast, United Kingdom

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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RECONFIGURABLE ACCELERATORS MEET HETEROGENEOUS ARCHITECTURES

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): SoC, Heterogeneous, and Reconfigurable Architectures

Room: 3006, 3rd Floor

Session Chair(s): Linghao Song, University of California, Los Angeles; Andreas Guerreri, École Polytechnique Fédérale de Lausanne

Heterogeneous systems combine application software with specialized hardware modules. This session presents the state of the art for promising heterogeneous architectures including algorithm/hardware co-design, coarse-grained reconfigurable arrays, and GPUs. Memory management plays a critical role in such systems to unleash their potential performance. Clever optimizations such as data-reuse-friendly designs, elastic FIFOs, unified virtual memory, and die-stacked hybrid memory architectures are presented in this session, showing new ways to meet ever-increasing efficiency demands.

LIGHTNING TALK – HETEROGENEOUS RECONFIGURABLE ACCELERATORS: TRENDS AND PERSPECTIVES

Wayne Luk, Imperial College London, United Kingdom

HDSUPER: ALGORITHM-HARDWARE CO-DESIGN FOR LIGHT-WEIGHTED HIGH-QUALITY SUPER RESOLUTION ACCELERATOR

Liang Chang, Xin Zhao, Dongqi Fan, Zhicheng Hu, Jun Zhou, University of Electronic Science and Technology of China, Chengdu, China

DARIC: A DATA REUSE-FRIENDLY CGRA FOR PARALLEL DATA ACCESS VIA ELASTIC FIFOs

Dajiang Liu, Di Mou, Rong Zhu, Yan Zhuang, Jiaying Shang, Jiang Zhong, Shouyi Yin, Chongqing University, Chongqing, China

ORCHESTRATED SCHEDULING AND PARTITIONING FOR IMPROVED ADDRESS TRANSLATION IN GPUS

Bingyao Li, Yueqi Wang, Xulong Tang, University of Pittsburgh, PA

BUMBLEBEE: A MEMCACHE DESIGN FOR DIE-STACKED AND OFF-CHIP HETEROGENEOUS MEMORY SYSTEMS

Yifan Hua, Shengan Zheng; Ji Yin, Weidong Chen, Linpeng Huang, Shanghai Jiao Tong University, Shanghai, China

WHEN BIO-INSPIRED MODELS MET HARDWARE OPTIMIZATION

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): Emerging Models of Computation

Room: 3010, 3rd Floor

Session Chair(s): Priyadarshini Panda, Yale University; Haowen Fang, Synopsys

This session presents non-conventional hardware architecture for neural-inspired computing models. The first paper explores design space optimization of asynchronous neuromorphic hardware, the second and third papers discuss optimization of neuromorphic computing using in-memory computing, and the last paper addresses acceleration of graph processing, which is the base of many neuromorphic computing models.

LIGHTNING TALK – A PERSPECTIVE ON NEUROMORPHIC COMPUTING

Kaushik Roy, Purdue University, West Lafayette, IN

ANAS: ASYNCHRONOUS NEUROMORPHIC HARDWARE ARCHITECTURE SEARCH BASED ON SYSTEM-LEVEL SIMULATOR

Jian Zhang, Jilin Zhang, Dexuan Huo, Hong Chen, Tsinghua University, Beijing, China

INPUT-AWARE DYNAMIC TIMESTEP SPIKING NEURAL NETWORKS FOR EFFICIENT IN-MEMORY COMPUTING

Yuhang Li, Abhishek Moitra, Tamar Geller, **Priyadarshini Panda**, Yale University, New Haven, CT

NEUROMORPHIC SWARM ON RRAM COMPUTE-IN-MEMORY PROCESSOR FOR SOLVING QUBO PROBLEM

Ashwin Sanjay Lele, Muya Chang, Samuel Spetalnick, Brian Crafton, Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA; **Yan Fang**, Kennesaw State University, Marietta, GA

ACGRAPH: ACCELERATING STREAMING GRAPH PROCESSING VIA DEPENDENCE HIERARCHY

Zihan Jiang, Fubing Mao, Yapu Guo, Xu Liu, Haikun Liu, Xiaofei Liao, Hai Jin, Jin Zhao, Huazhong University of Science and Technology, Wuhan, China; Wei Zhang, Hong Kong University of Science and Technology, Hong Kong

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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IS DEEP LEARNING COMPUTATIONALLY SUSTAINABLE?

Time: 10:30 AM – 12:00 PM

Event Type: Research Panel

Topic Area(s): AI

Room: 3014, 3rd Floor

Organizer/Moderator: Swagath Venkataramani, IBM, West Lafayette, IN

The past decade witnessed the advent and rapid growth of “deep” AI models that have achieved super-human levels of accuracy on many complex tasks involving images, video, text and natural language. Their emergence continues to shape the application landscape---many industries spanning mission-critical domains (self-driving, banking, healthcare) to recommendation systems (web search, chat bots, digital assistant) have infused deep AI in their products and services with commercial success. This has resulted in an urgent need to deploy AI models at scale and across computing devices from datacenters/cloud to edge/IoT devices, each bringing their unique sets of challenges.

The success of deep AI models can be primarily attributed to scale—the scale (number of parameters, layers) of the model, the scale of data on which they are trained. AI models with hundreds of millions to billions of parameters are becoming commonplace and models with trillions of parameters have successfully prototyped. As the AI models scale, so does their compute requirements! The demand for compute has far outpaced the traditional approaches to compute scaling and this forms the basis for the central question the panel explores: “Is Deep Learning computationally sustainable?”

The panel will encourage discussion on multiple (and equally viable) points-of-views from the experts on this topic. The first point-of-view would delve into promising directions to improve the compute efficiency of deep learning which would make it computationally sustainable. This includes research directions such as hardware acceleration, approximate computing and others. Another perspective, which is a step change from traditional deep learning, is to embrace the use foundation models. In this case, pre-training large foundation models is still costly and requires large corpus of data, but they can be fine-tuned at a relatively cheaper cost and with little labeled data for individual tasks. A more radical perspective would seek newer learning methods which are not based on backpropagation. Bio-inspired learning methods, neuro-symbolic AI and Hyper-dimensional (HD) computing fall in this category. Overall, the panel will seek to bring out these divergent viewpoints on how deep learning should evolve for it to be computationally sustainable.

This panel brings together the foremost experts from industry and academia with experience in building and deploying computing systems for deep learning. The panel will be structured to bring out the key computational challenges and the experts’ viewpoints on how AI systems of the future will be designed and deployed.

Panelists: Jan Rabaey, University of California, Berkeley, CA; David Patterson, Google, Mountain View, CA; Diana Marculescu, The University of Texas at Austin, TX; Pradeep Dubey, Intel, Cupertino, CA; Brucek Khailany, NVIDIA, Austin, TX

DESIGN THE CLOUDS: ACCELERATION, INTERCONNECT, AND INFRASTRUCTURE

Time: 10:30 AM – 12:00 PM

Event Type: Special Session (Research)

Topic Area(s): AI, Cloud

Room: 3001, 3rd Floor

Organizer(s): Jingtong Hu, University of Pittsburgh; Peipei Zhou, University of Pittsburgh

Cloud computing is an increasingly popular way to use computing and storage technologies, and it is changing the way businesses deliver services. In order to provide scalable, reliable, secure, and cost-effective services, including machine learning, Searching, FinTech, etc., service providers need to constantly innovate the hardware infrastructure design in the Clouds. In this Special Session, we have three speakers from Intel, Microsoft, and Google to talk about their latest progress in achieving energy-efficient, secure, and reliable hardware infrastructures, which covers Interconnect designs, Infrastructure Processing Units (IPUs), and TPUs.

COMPUTE EXPRESS LINK (CXL*): OPEN INTERCONNECT FOR CLOUD INFRASTRUCTURE

Debendra Das Sharma, Intel, Santa Clara, CA

MOVING THE CENTER OF CLOUD SERVERS FROM PROCESSORS TO IPUS

Derek Chiou, Microsoft, The The University of Texas, Austin, TX

CODESIGN FROM SEMICONDUCTORS TO AI

Cliff Young, Google, Mountain View, CA

WHAT CHATGPT AND GENERATIVE AI MEANS FOR SEMICONDUCTOR DESIGN AND DEVELOPMENT

Time: 11:30 AM – 12:30 PM

Event Type: TechTalk

Topic Area(s): AI

Room: DAC Pavilion, Level 2 Exhibit Hall

ChatGPT has generated a lot of excitement and speculation lately. People are asking how generative AI will affect us all. Questions around generative AI’s potential and limitations are top of mind.

This talk will touch on how AI/ML is helping in the semiconductor industry, and what generative AI can do for the chip design process. How it is likely to affect how we build chips, and what it could mean for semiconductor productivity.

Presenter: Erik Berg, Microsoft

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

THE CEREBRAS CS-2: DESIGNING AN AI ACCELERATOR AROUND THE WORLD'S LARGEST 2.6 TRILLION TRANSISTOR CHIP

Time: 1:00 PM – 1:45 PM

Event Type: SKYTalk

Topic Area(s): AI

Room: DAC Pavilion, Level 2 Exhibit Hall

Today's exponential growth of neural networks is creating a demand for compute infrastructure that can't keep up with the traditional performance improvements gained through enhancements of semiconductors technology nodes. A co-designed approach is needed to keep up with the demand. We explore how increasing chip dimensions and resulting power and cooling densities are some of the enabling vectors of such co-design.

Presenter: Jean-Philippe Fricker, Cerebras, Santa Clara, CA

ALTERNATIVE APPROACHES TO AI CHIP ARCHITECTURES

Time: 1:00 PM – 1:45 PM

Event Type: Transformative Technologies Theater

Topic Area(s): AI

Room: Transformative Technologies Theater, Level 1 Exhibit Hall

The field of artificial intelligence has seen significant advancements in recent years, largely driven by the development of novel hardware architectures that can support the massive computational demands of AI algorithms. However, many of the current chip architectures are limited in their ability to handle the growing complexity of AI workloads, and alternative approaches are needed to further improve performance and energy efficiency.

This panel will explore several alternative approaches to AI chip architectures that have emerged in recent years. These include, but are not limited to, at-memory vs in-memory computing vs von-Neumann, SoCs vs accelerators, purpose built inference chips versus training/ inference chips. Each of these approaches offers unique advantages over traditional CPU-based architectures, such as improved energy efficiency, lower latency, and higher throughput.

Panelist will discuss the advantages of these approaches, as well as potential applications in various domains, such as image and speech recognition, natural language processing, and robotics. The panel will provide a comprehensive overview of the state-of-the-art in AI chip architectures and stimulate discussions on the future directions of this rapidly evolving field.

Moderator: Sally Ward-Foxton, EE-Times, London, United Kingdom

EDGE – AI AND SECURITY

Time: 1:30 PM – 3:00 PM

Event Type: Engineering Tracks

Topic Area(s): Embedded Systems and Software

Room: 2010, 2nd Floor

Organizer(s): ChengYeh Wang, MediaTek, Hsinchu City, Taiwan;

This session will discuss the advancements in Edge AI and the challenges of developing high-performance, low-latency systems that can handle advanced models, and provide increased flexibility and methods to protect Model IP. Additionally, we will delve into the subject of secure and efficient updates and control in the field for Edge Devices, as well as the concept of a device lifecycle to facilitate manufacturing, deployment, and management. The session will examine this topic from multiple perspectives, including device user, OEM/device provider, and silicon provider. However, security and memory corruption vulnerabilities have been extensively studied but lack universal mitigation strategies for deeply embedded and functional-safety-relevant systems. We will explore binary translation – a practical software technique to protect embedded systems.

Presenters: Nicusor Penisoara, NXP Semiconductors, Valbonne, France; Rehan Hameed, Kinara.ai, San Francisco, CA; Tim Blazytko, Emproof BV, Bochum, Germany

DAC SYSTEM DESIGN CONTEST 2023 – FINALIST PRESENTATIONS

Time: 1:30 PM – 3:00 PM

Topic Areas: Design, EDA

Room: 2008, Level 2

Organizing(s): Jeff Goeders, Brigham Young University; Calli Hao, Georgia Institute of Technology; Meng Li, Peking University; Cheng Zhou, Zhejiang University

The DAC System Design Contest focuses on object detection and classification on an embedded GPU or FPGA system. Contestants will receive a training dataset provided by Baidu, and a hidden dataset will be used to evaluate the performance of the designs in terms of accuracy and speed. Contestants will compete to create the best performing design on a Nvidia Jetson Nano GPU or Xilinx Kria KV260 FPGA board. Grand cash awards will be given to the top three teams.

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

ADVANCED IP – GROUNDBREAKING RESULTS

Time: 1:30 PM – 3:00 PM
Event Type: Engineering Tracks
Topic Area(s): IP
Room: 2012, 2nd Floor

Session Chair(s): Henning Spruth (NXP Semiconductors)
 Differentiating advanced IP is a critical challenge in today's environment. Can high-performance RISC V IP run at low power? How can architectures be optimized to enable hyperspace AI models? How can users achieve scalability for CNN architectures in FPGA implementations? How can chiplet and die-to-die (D2D) interfaces meet interoperability challenges? How can IP be developed to address advanced clock and DC challenges? This session will show the latest groundbreaking results from IP development, emphasizing critical implementation and verification considerations that helped achieve those results.

WORLD FASTEST & MOST POWER EFFICIENT RISC-V

Andy Huang, *Micro Magic Inc., Cupertino, CA*

CHIPLET AND DIE-TO-DIE (D2D) INTERFACE INTEROPERABILITY-HOW TO ACCELERATE THE PATH TO AN OPEN ECOSYSTEM

Letizia Guiliano, *Alphawave Semi, Portland, OR*; **Clint Walker**, *Alphawave*

A FREQUENCY OPTIMIZED LINEAR SCALABLE ARCHITECTURE FOR CNN IMPLEMENTATION ON FPGAS

Nanditha Rao, *Indian Institute of Information Technology, Bangalore, India*

A NOVEL IP FOR REAL TIME DC ESTIMATION AND REMOVAL

Ankur Bal, *STMicroelectronics, Greater Noida, India*; **Vikram Singh**, *STMicroelectronics, Noida, India*

AN AUTOMATIC INPUT CLOCK DUTY-RANGE EXTENDER CIRCUIT TO BE USED AS PART OF A CLOCK DUTY-CYCLE ADJUSTER CIRCUIT

Ayan Dutta, *OpenFive, Bengaluru, India*

LATENCY PROCESSING UNIT (LPU) FOR ACCELERATION OF HYPERSCALE AI MODELS

Joo-Young Kim, **Seongmin Hong**, **Seungjae Moon**, **Jung-Hoon Kim**, **Junsoo Kim**, **Junseo Cha**, **Gyubin Choi**, **Sekyong Song**, *HyperAccel, Daejeon, South Korea*

AI A GOLDMINE FOR ATTACKERS

Time: 1:30 PM – 3:00 PM
Event Type: Research Manuscript
Topic Area(s): AI/ML Security/Privacy
Room: 3004, 3rd Floor

Session Chair(s): Jeyavijayan Rajendran, Texas A&M University; Ning Zhang, Washington University, St. Louis

Exploring the Vulnerabilities of AI Systems: Opportunities and Challenges for Security Researchers is the theme of this session. It will delve into the world of artificial intelligence (AI) from a security perspective. AI has proven to be a gold mine for security researchers due to the many manipulation possibilities it presents. This session will provide an in-depth exploration of various attacks and bypassing techniques that can be used against AI systems. Attendees will gain a deeper understanding of the current state of AI security and the types of attacks that are most common in the field.

This session will present three research papers on machine learning and security topics. The first paper, HyperAttack, is a novel attack framework for HDC models that degrades accuracy by maliciously flipping a few bits in its memory system. The second paper, MPass, is a hard-label black-box attack on ML-based detectors that uses explainability to modify critical positions in malware and maintain functionality. The third paper, VideoFlip, highlights the first hardware-based fault-injection attack on video compression, capable of altering a few bits to increase the bitrate or degrade video quality.

LIGHTNING TALK – AI A GOLDMINE FOR ATTACKERS

Siddharth Garg, *Brooklyn, NY*

MPASS: BYPASSING LEARNING-BASED STATIC MALWARE DETECTORS

Jialai Wang, **Yi Rong**, **Han Qiu**, **Qi Li**, **Zongpeng Li**, **Chao Zhang**, *Tsinghua University, Beijing, China*; **Wenjie Qu**, *Huazhong University of Science and Technology, Chaoyang, China*

VIDEOFLIP: ADVERSARIAL BIT-FLIPS FOR REDUCING VIDEO SERVICE QUALITY

Jung-Woo Chang, **Mojan Javaheripi**, **Farinaz Koushanfar**, *University of California, San Diego, CA*

HYPERATTACK: AN EFFICIENT ATTACK FRAMEWORK FOR HYPERDIMENSIONAL COMPUTING

Fangxin Liu, **Haomin Li**, **Yongbiao Chen**, **Tao Yang**, **Li Jiang**, *Shanghai Jiao Tong University, Shanghai, China*

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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DO YOU KNOW WHAT YOU WILL GET FROM LITHOGRAPHY?

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): Design for Manufacturing and Reliability

Room: 3008, 3rd Floor

Session Chair(s): Iris Hui-Ru Jiang, National Taiwan University
Takashi Sato, Kyoto University

In the path towards more cost-efficient semiconductor processes, the necessary transformation of layout features to mask shapes is increasingly less intuitive and requires more sophisticated methods for layout compliance. In this session, the first two papers present how to accelerate inverse lithography by complex-valued neural fields and a multi-level approach. In addition, the last two papers present layout-compliant methods for two different directed self-assembly process implementations, with one targeting interconnects and the other targeting vias.

LIGHTNING TALK – LITHOGRAPHY AND ADVANCED TECHNOLOGIES WORK TOGETHER TO DELIVER THE FOUNDRY’S NEEDS

Charles Chiang, Synopsys, Saratoga, CA

PHYSICS-INFORMED OPTICAL KERNEL REGRESSION USING COMPLEX-VALUED NEURAL FIELDS

Guojin Chen, Zehua Pei, Bei Yu, Martin Wong, The Chinese University of Hong Kong; Haoyu Yang, NVIDIA, Austin, TX; Yuzhe Ma, The Hong Kong University of Science and Technology, Guangzhou, China

EFFICIENT ILT VIA MULTI-LEVEL LITHOGRAPHY SIMULATION

Shuyuan Sun, Fan Yang, Li Shang, Xuan Zeng, Fudan University, Shanghai, China; Bei Yu, The Chinese University of Hong Kong, Shatin, Hong Kong

GRAPH-BASED SIMULTANEOUS PLACEMENT AND ROUTING FOR TWO-DIMENSIONAL DIRECTED SELF-ASSEMBLY TECHNOLOGY

Wei-Hsu Chen, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

LAMELLAR DSA-AWARE DETAILED ROUTING CONSIDERING DOUBLE PATTERNING AND SHORT TEMPLATE MINIMIZATION

Kuei-Lin Wu, Shao-Yun Fang, National Taiwan University of Science and Technology, Taipei, Taiwan

FRESH PERSPECTIVES IN AI SYSTEM DESIGN

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML System and Platform Design

Room: 3003, 3rd Floor

Session Chair(s): Ramtin Mohammadizand, University of South Carolina

As new AI application and technology emerges, there are new considerations and metrics needed when designing AI systems. In this session, we will learn about these fresh perspectives, including an automatic framework for AI fairness, adversarial training optimization, new metrics for accuracy/hyperparameter exploration for Compute-In-Memory (CIM) accelerators, and the roughness problem in Diffractive Optical Neural Networks (DONNs).

LIGHTNING TALK – ARCHITECTURE 2.0

Vijay Janapa Reddy, Harvard University, Cambridge, MA

MUFFIN: A FRAMEWORK TOWARD MULTI-DIMENSION AI FAIRNESS BY UNITING OFF-THE-SHELF MODELS

Yi Sheng, Junhuan Yang, Lei Yang, Weiwen Jiang, George Mason University, Fairfax, VA; Yiyu Shi, University of Notre Dame, South Bend, IN; Jingtong Hu, University of Pittsburgh, PA

FAST ADVERSARIAL TRAINING WITH DYNAMIC BATCH-LEVEL ATTACK CONTROL

Jaewon Jung, Jaeyong Song, Hongsun Jang, Hyeyoon Lee, Kanghyun Choi, Noseong Park, Yonsei University, Seoul, South Korea; Jinho Lee, Seoul National University, Seoul, South Korea

UNIFIED AGILE ACCURACY ASSESSMENT IN COMPUTING-IN-MEMORY NEURAL ACCELERATORS BY LAYERWISE DYNAMICAL ISOMETRY

Xuan-Jun Chen, Cynthia Kuan, Chia-Lin Yang, National Taiwan University, Taipei, Taiwan

PHYSICS-AWARE ROUGHNESS OPTIMIZATION FOR DIFFRACTIVE OPTICAL NEURAL NETWORKS

Shanglin Zhou, Zhijie Shi, Caiwen Ding, University of Connecticut, Storrs, CT; Yingjie Li, Minhan Lou, Weilu Gao, Cunxi Yu, University of Utah, Salt Lake City, UT

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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INVESTIGATING DATA FOR DNN ACCELERATION!

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Architecture Design

Room: 3006, 3rd Floor

Session Chair(s): Youngsoo Shin, Korea Advanced Institute of Science and Technology (KAIST); Joon-Sung Yang, Yonsei University

This session highlights various algorithm/design approaches and accelerators for AI/ML. Four papers are presented to highlight acceleration for graph processing, training with near-memory processing and bit-serial inference.

LIGHTNING TALK – EDA WITH ML, RULE-BASED, OR BOTH?

Youngsoo Shin, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea

PSMINER: A PATTERN-AWARE ACCELERATOR FOR HIGH-PERFORMANCE STREAMING GRAPH PATTERN MINING

Hao Qi, Yu Zhang, Jun Huang, Haoyu Lu, Jin Zhao, Hai Jin, Huazhong University of Science and Technology, Wuhan, China; Ligang He, University of Warwick, Coventry, United Kingdom; Kang Luo, Huazhong University of Science and Technology

INSTANT-NERF: INSTANT ON-DEVICE NEURAL RADIANCE FIELD TRAINING VIA ALGORITHM-ACCELERATOR CO-DESIGNED NEAR-MEMORY PROCESSING

Yang Zhao, Shang Wu, Jingqun Zhang, Sixu Li, Chaojian Li, Yingyan (Celine) Lin, Georgia Institute of Technology, Atlanta, GA

BIT-SERIAL CACHE: EXPLOITING INPUT BIT VECTOR REPETITION TO ACCELERATE BIT-SERIAL INFERENCE

Yun-Chen Lo, Ren-Shuo Liu, National Tsing Hua University, Hsinchu, Taiwan

SAGRAPH: A SIMILARITY-AWARE HARDWARE ACCELERATOR FOR TEMPORAL GRAPH PROCESSING

Jin Zhao, Yu Zhang, Jian Cheng, Yiyang Wu, Chuyue Ye, Hui Yu, Zhiying Huang, Hai Jin, Xiaofei Liao, Lin Gu, Haikun Liu, Huazhong University of Science and Technology, Wuhan, China

NEW WAVES OF BOOSTING POWER EFFICIENCY

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): Timing and Low Power Design

Room: 3002, 3rd Floor

Session Chair(s): Qi Sun, Cornell University; Zhou Jin, China University of Petroleum

This session describes four methods of boosting the power, energy, and thermal performances. It opens with an operator learning based technique to boost the performance of thermal simulation. The next presentation describes the investigation of tensor processing unit and the control of timing error. The third presentation describes a novel power meter design to prevent power spikes for DNN. Finally, the session closes with a cache mitigation technique to enable thermal safety.

LIGHTNING TALK – POWER AND PERFORMANCE RECONCILIATION – FROM TRADEOFF TO WIN-WIN

Jiang Hu, Texas A&M University, College Station, TX

DEEPOHEAT: OPERATOR LEARNING-BASED ULTRA-FAST THERMAL SIMULATION IN 3D-IC DESIGN

Ziyue Liu, Xinling Yu, Zheng Zhang, University of California, Santa Barbara, CA; Yixing Li, Zhiyu Zeng, Cadence Design Systems, Inc., Austin, TX; Jing Hu, Shinyu Shiao, Xin Ai, Cadence Design Systems, Inc., San Jose, CA

STRIVE: ENABLING CHOKE POINT DETECTION AND TIMING ERROR RESILIENCE IN A LOW-POWER TENSOR PROCESSING UNIT

Noel Daniel Gundi, Zinnia Muntaha Mowri, Andrew Chamberlin, Sanghamitra Roy, Koushik Chakraborty, Utah State University, Logan, UT

PROPHET: PREDICTIVE ON-CHIP POWER METER FOR HARDWARE DNN ACCELERATOR

Jian Peng, Tingyuan Liang, Zhiyao Xie, Wei Zhang, Hong Kong University of Science and Technology, Hong Kong

MACHINE LEARNING-BASED THERMALLY-SAFE CACHE CONTENTION MITIGATION IN CLUSTERED MANYCORES

Mohammed Bakr Sikal, Heba Khdr, Martin Rapp, Joerg Henkel, Karlsruhe Institute of Technology, Karlsruhe, Germany

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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NOT FAST ENOUGH? HARDWARE ACCELERATION FOR TRANSFORMERS AND BEYOND

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Architecture Design

Room: 3012, 3rd Floor

Session Chair(s): Younghyun Kim, University of Wisconsin, Madison; Sumit Mandal, Indian Institute of Science

The complexity of new deep learning techniques continues to grow at unprecedented speeds, making programmable solutions stagnant. Hardware acceleration can come to the rescue, but the immense complexity either cripples the performance or explodes the area cost. The papers in this session present innovative techniques to exploit the structure, memory access patterns, and statistical properties of these algorithms toward superior efficiency. These solutions pave the way to natural language processing and computer vision applications not possible today.

LIGHTNING TALK – BIGGER AND SMARTER: SCALE UP YOUR AI ACCELERATORS

Yu Cao, Arizona State University, Tempe, AZ

*COSA: CO-OPERATIVE SYSTOLIC ARRAYS FOR MULTI-HEAD ATTENTION MECHANISM IN NEURAL NETWORK USING HYBRID DATA REUSE AND FUSION METHODOLOGIES

Zhican Wang, Gang Wang, Honglan Jiang, Ningyi Xu, Guanghui He, Shanghai Jiao Tong University, Shanghai, China

TF-MVP: NOVEL SPARSITY-AWARE TRANSFORMER ACCELERATOR WITH MIXED-LENGTH VECTOR PRUNING

Eunji Yoo, Gunho Park, Jung Gyu Min, Youngjoo Lee, Pohang University of Science and Technology (POSTECH), Pohang, South Korea; Se Jung Kwon, Baeseong Park, Dongsoo Lee, NAVER Cloud, Seoul, South Korea

EFFICIENT TRANSFORMER INFERENCE WITH STATICALLY STRUCTURED SPARSE ATTENTION

Steve Dai, NVIDIA, Santa Clara, CA; Hasan Genc, University of California, Berkeley, CA; Rangharajan Venkatesan, NVIDIA, San Jose, CA; Brucek Khailany, NVIDIA, Austin, TX

UNLEASHING THE POWER OF NEURAL NETWORKS THROUGH HARDWARE ACCELERATION

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): SoC, Heterogeneous, and Reconfigurable Architectures

Room: 3010, 3rd Floor

Session Chair(s): Yingyan Lin, Rice University; Ganapati Bhat, Washington State University

Artificial Neural Networks (NNs) have found widespread application in almost every aspect of our daily lives. While the longtime showstopper, i.e., the training, has seen major breakthroughs in recent years, efficient custom hardware implementations are still in the process of taking NN adoption to the next level. This session covers novel approaches in the areas of mapping NNs to heterogeneous architectures, co-designing NPUs and ASIPs, NoC-based NN accelerators with distributed buffers, and a multi-output Monte Carlo dropout-based Bayesian NN, along with a tool to generate FPGA-based accelerators for them.

LIGHTNING TALK: CHALLENGES OF MAPPING GNN'S AND DNN'S WITH LIMITED MEMORY

Arvind Mithal, Massachusetts Institute of Technology, Cambridge, MA

MEMORY AND COMPUTATION COORDINATED MAPPING OF DNNs ONTO COMPLEX HETEROGENEOUS SOC

Size Zheng, Siyuan Chen, Yun (Eric) Liang, Peking University, Beijing, China

APPEND: TOWARDS APPLICATION ENHANCED NPU DESIGNING

Cangyuan Li, Ying Wang, Huawei Li, Yinhe Han, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

VENUS: A VERSATILE DEEP NEURAL NETWORK ACCELERATOR ARCHITECTURE DESIGN FOR MULTIPLE APPLICATIONS

Jiaqi Yang, Ahmed Louri, George Washington University, Washington, DC; Hao Zheng, University of Central Florida, Orlando, FL

WHEN MONTE-CARLO DROPOUT MEETS MULTI-EXIT: OPTIMIZING BAYESIAN NEURAL NETWORKS ON FPGA

Hongxiang Fan, University of Cambridge, United Kingdom; Mark Chen, Liam Castelli, Zhiqiang Que, Kenneth Long, Wayne Luk, Imperial College London, London, United Kingdom; He Li, Southeast University, Nanjing, China

* Denotes a Best Paper Candidate

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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LOST IN SILICON: THE NEED FOR RE-INNOVATING THE FUTURE OF TRUSTED HARDWARE AND SUPPLY CHAIN RESILIENCE

Time: 1:30 PM – 3:00 PM

Event Type: Research Panel

Topic Area(s): Security

Room: 3014, 3rd Floor

Organizer(s): Ahmad-Reza Sadeghi, Technische Universität Darmstadt, Hessen, Germany; Jeyavijayan Rajendran, Texas AM University, College Station, TX

The desire to establish digital sovereignty, the recent global semiconductor shortages, and geopolitical interests are driving forces behind various worldwide initiatives to strengthen semiconductor technology and manufacturing on a national and regional basis. Hardware is at the heart of all computing systems; hence, trustworthy and reliable hardware is essential. Otherwise, critical systems and supply chains will be at risk.

However, in recent years, we are witnessing the discovery of a growing number of hardware design and implementation vulnerabilities exploited by unprivileged software, exposing sensitive data or compromising the underlying computing platforms. This new attack paradigm casts a long shadow on decades of research on system security. It disrupts the traditional threat models that focus mainly on software-only vulnerabilities and often assume that the underlying hardware is behaving correctly and is trustworthy. Unfortunately, existing solutions are often ad-hoc, limited, inefficient, and address only specific problems.

The goal of this interactive panel is to bring together leading international researchers and experts from academia, industry, and government and discuss the challenges related but not limited to, themes such as

- security-by-design for hardware and supply chains,
- scalable assurance and trust-establishment methodologies for hardware security and resilience,
- security-aware electronic design automation.

Moderator: Jeyavijayan Rajendran, Texas A&M University, College Station, TX; Ahmad-Reza Sadeghi, Technische Universität, Darmstadt, Hessen, Germany

Panelists: Jon Azen, Qualcomm, San Diego, CA; Sanjay (Jay) Rekhi, NIST; Mike Borza, Synopsys, Ottawa, Canada; Gang Qu, University of Maryland, College Park, MD; Farinaz Koushanfar, University of California, San Diego, CA

TINYML: BRING DEEP LEARNING MODELS TO TINY DEVICES

Time: 1:30 PM – 3:00 PM

Event Type: Special Session (Research)

Topic Area(s): AI

Room: 3001, 3rd Floor

Organizer(s): Mimi Xie, The The University of Texas at San Antonio

Tiny Machine learning (TinyML) is an increasingly growing field that enables intelligent algorithms on tiny edge devices with extremely limited resources. The advances of TinyML have opened up new opportunities for designing smart applications ranging from medical care devices, environmental monitoring, to critical infrastructure monitoring and protection by embedding intelligence into ubiquitous devices and performing on-device sensor data analytics and decision making. This session features three experts from academia and industry in the field of TinyML with expertise on intelligent sensors, hardware/software codesign frameworks, and chip design for tiny machine learning system. The challenges in on-device intelligence, open research opportunities, and emerging applications will be highlighted in the domain of TinyML.

MACHINE LEARNING SENSORS: BUILDING BLOCKS FOR AI-ENABLED SYSTEMS

Pete Warden, Stanford University, Stanford, CA

ALGORITHM-SOFTWARE-HARDWARE CO-DESIGN FOR DEEP LEARNING ACCELERATION

Yanzhi Wang, Northeastern University, Boston, MA

CROSS-LAYER INNOVATIONS FOR ENABLING REAL-TIME AND EFFICIENT EYE TRACKING IN VR/AR

Yingyan (Celine) Lin, Georgia Institute of Technology, Atlanta, GA

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

IS SYSTEMS ENGINEERING THE SOLUTION TO THE LIMITS OF DENNARD SCALING AND MOORE'S LAW?

Time: 2:00 PM – 2:45 PM

Event Type: DAC Pavilion Panel

Topic Area(s): Design

Room: DAC Pavilion, Level 2 Exhibit Hall

With the increasing semiconductor content in multi-domain systems, the overall system characteristics are largely determined by the overlap of SoC and physical systems. In a software-defined world, the systems themselves become a constant tradeoff between the Physical, Semiconductor, and Software worlds, whether we're talking about an SoC, autonomous vehicle, or automated factory.

As such, the biggest optimizations available to systems engineers will be in the overlap between the different system contexts – be it block, SoC, HW/SW, Module, Board, or system. Such optimizations have the potential to provide benefits that are significantly larger than the localized optimizations we have been relying on. Realizing these gains however introduces its own challenges and the need for additional tools and analysis that can look across these contexts and domains, as well as bring together a diverse set of people that do not normally work together within a consistent system view.

The panel will examine what these new requirements are if they should come from traditional system design practices or new capabilities that understand EDA and HW/SW at its core, and if a new skill set and persona is needed within systems engineering to enable success. Additionally, we will examine what impact recent industry consolidation will have on both the needs of the systems designers (consolidation in the system space) as well as on the enabling technologies (consolidation in the tool vendors).

Moderator: Alix Paultre, Endeavor B2B, Weisbaden, Germany

Panelists: Mark Malinoski, Siemens EDA, Portland, OR; Pooria Yaghini, SpaceX; Larry Williams, Ansys; Brett Hillhouse, IBM

THE INDUSTRY 4.0 REVOLUTION OF SEMICONDUCTOR DESIGN

Time: 3:00 PM – 3:45 PM

Event Type: DAC Pavilion Panel

Topic Area(s): Design

Room: DAC Pavilion, Level 2 Exhibit Hall

The fourth industrial revolution, also known as Industry 4.0, has brought significant changes to manufacturing processes and supply chains across many industries. It is described as the ongoing transformation of traditional development and industrial practices through advanced technologies such as automation, AI, IoT, cloud computing, and big data analytics. Industry 4.0 involves the digitalization and interconnection of all aspects in the value chain, leading to optimization, efficiency, and scale.

In this panel discussion, we will explore the implications of Industry 4.0 on semiconductor design and development, including readiness of the industry to adopt these new technologies. We will explore the unification of value chain stages, bringing test and lifetime operation closer to the design for enhanced learning and collaboration. By adopting emerging techniques that rely on machine learning, cloud analytics, remote diagnostics, and predictive modeling, the semiconductor industry can resume efficient and effective decision-making – with great potential impact on revenue growth for semiconductor companies. We will also examine the hurdles that the industry must overcome to fully enable Industry 4.0, including challenges related to data management, security, and interoperability. The panel will consist of experts from various segments of the semiconductor industry and through this discussion, we hope to provide valuable insights into the current state of the industry and the opportunities and challenges presented by Industry 4.0.

The adoption of Industry 4.0 technologies has the potential to revolutionize industries and businesses, resulting in increased productivity, reduced costs, improved product quality, and enhanced customer experiences. Is the semiconductor industry ready for it?

Key questions:

- What does industry 4.0 mean for semiconductor design and production?
- Is the semiconductor industry ready to adopt industry 4.0?
- What technologies are crucial to successfully enable industry 4.0 throughout the semiconductor design and development stages?
- What is the potential impact on revenue growth for semiconductor companies?
- What are the hurdles that the industry must overcome to fully enable industry 4.0?
- What will it take to build trust in these new approaches?

Moderator: Brian Bailey, Semiconductor Engineering, Beaverton, OR

Panelists: Vijay Narayanan, proteanTecs, Milpitas, CA; Mujtaba Hamid, Microsoft, Redmond, WA; KT Moore, Cadence Design Systems, Inc., Rockwall, TX; Mohit Gupta, Alphawave Semi, Portland, OR

Research Sessions

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Engineering Track

PHYSICAL DESIGN CHALLENGES MANIFESTED

Time: 3:30 PM – 5:00 PM

Event Type: Engineering Tracks

Topic Area(s): Back-End Design

Room: 2008, Level 2

Session Chair(s): Greg Ford, Marvell Technology

We understood the Language of your Mind. Settle in for some insights to overcome physical design obstacles with these automation techniques to get to the other side of the corn field maze!

ACCELERATED DESIGN CONVERGENCE USING AUTOMATIC RECIPE TUNING THROUGH INTEL ENABLED AI-ML PNR FRAMEWORK

Rohit Kumar, Jagadeesh Boddu, Intel, Karnataka, India; **Raghavendra Vasappanavara**, Intel, San Diego, CA; Narendra Nimmagadda, Intel, Fishers, IN

ML BASED DRV PREDICTION AND OPTIMIZATION FOR DTCO

Mintae Lee, Wook Kim, Naya Ha, Samsung Electronics, Hwaseong, South Korea

OVER-DESIGN METHODOLOGY FOR OPERATING VOLTAGE MINIMIZATION

Joohee Choung, Samsung Electronics, Hwaseong, South Korea

ACHIEVE DATAFLOW AND GLOBAL PLACEMENT COHERENCE USING VIRTUAL OBJECT CONSTRAINT

Jing Wang, Yang Liu, Zixiao Wang, Qiuling Zeng, HiSilicon, Shenzhen, China; **Dmitry Yakimets**, Huawei, Leuven, Belgium

PHYSICAL IMPLEMENTATION AND ANALYSIS OF FUNCTIONAL SAFETY FEATURES (FUSA) IN AUTOMOTIVE CHIPS

Shashikiran Srinivasa, Badri Ramasubramanian, Pavan Kudumula, Marvell, Bangalore, India; **Atul Bhattarai**, Marvell, Santa Clara, CA

MULTI-CYCLE INTERCONNECT SYNTHESIS (MCIS): (DATA) REGISTER TREE CONSTRUCTION

Nancy Zhou, IBM, Cedar Park, TX; Gi-Joon Nam, Jinwook Jung, **Lakshmi Reddy**, IBM Research, Yorktown, NY; Josiah Hamilton, Nany Kollesar, Gregory Shaeffer, IBM, Poughkeepsie, NY; Arjen Mets, IBM, Tarrytown, NY; Paul Villarrubia, IBM, Austin, TX; Nicolas Degors, IBM, Grenoble, France

CHIPLETS – THE NEW FRONTIER OF ELECTRONIC DESIGN! CHALLENGES AND SOLUTIONS IN CHIPLET-BASED DESIGNS

Time: 3:30 PM – 5:00 PM

Event Type: Engineering Tracks

Topic Area(s): Embedded Systems and Software

Room: 2010, 2nd Floor

Organizer(s): Moshe Zalcborg, Veriest Solutions Ltd., Petach Tikva, Israel

Chiplets are revolutionizing the industry. They enable modular products combining dies of different process nodes optimally selected for specific functions: Performance-driven processor chiplets at 3nm, interconnect chiplets at 5nm and SRAM/Caches at 7nm can be combined in one platform using 2.5D and 3D advanced packaging technologies. It also removes reticle barrier allowing chiplet-based products to exceed much reticle limit. High routing density and short interconnect distance enable product segmentation to chiplets with minimal area, power and latency overhead.

However, this also adds additional complexity to electronics design, both because of the sheer scale of integration, as well as the intricacies of interfacing different dies made by different players.

This session will review some of the challenges and possible solutions to those challenges.

Presenters: François Piednöel, Mercedes-Benz, Santa Clara, CA; Igor Elkanovich, Global UniChip Corp., Taipei, Taiwan; Andreas Olofsson, Zero ASIC, Boston, MA; Anunay Bajaj, Cadence Design Systems, Inc., Austin, TX

Research Sessions

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Keynotes and Visionary Talks

Engineering Track

SECURING IP IN THE CLOUD

Time: 3:30 PM – 5:00 PM

Event Type: Engineering Tracks

Topic Area(s): IP

Room: 2012, 2nd Floor

Session Chair(s): Rae Parnmukh (Google)

Chip design on cloud is growing rapidly, and almost all companies have (or should have!) a very coherent design-on-cloud strategy. Design on cloud has the potential to accelerate time to market by increasing design and verification velocity, especially when it comes to advanced node designs. There is no one-size-fits-all approach to designing on cloud. Some choose to migrate only certain workloads, while others may create additional tooling to burst to cloud seamlessly.

Regardless of the path to cloud, it is important to understand IP security on cloud. Cloud security ensures data and applications are available to authorized users. In this invited session, you will hear from multiple leaders on how teams are leverage the cloud successfully and SECURELY, and the best practices they follow and recommend.

TALK 1: ESTABLISHING TRUST IN IP THROUGH AUTOMATED ATTESTATION

Serge Leef, Microsoft, Bellevue, WA

TALK 2: SECURING IP IN THE CLOUD

Satish Govindappa, Synopsys, Tracy, CA; Bob Lefferts, Synopsys, Portland, OR; Mohan Mohan, Synopsys, Mountain View, CA

TALK 3: ENABLING BEST PRACTICES FOR DESIGN IN CLOUD

Paul Buenrostro, Western Digital, Irvine, CA

BEYOND MOORE IS COOL

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Emerging Device Technologies

Room: 3006, 3rd Floor

Session Chair(s): Kai Ni, Rochester Institute of Technology; Michael Niemier, University of Notre Dame

As the traditional 2D technology scaling is approaching the limit, many new opportunities arise in computing paradigms beyond Moore. This emerging device technologies session covers diverse topics of cryogenic CMOS and in-memory computing, thermal mitigation in 3D integrated circuits, and in-memory search using ferroelectric devices, as well as addressing security vulnerabilities in the NAND Flash.

LIGHTNING TALK – CREATIVE DESIGN BEYOND MOORE'S LAW

Damien Querlioz, Université Paris-Saclay, Paris, France

DESIGN AUTOMATION FOR CRYOGENIC CMOS CIRCUITS

Victor M. van Santen, Florian Klemme, Shivendra Parihar, University of Stuttgart, Germany; Marcel Walter, Robert Wille, Hussam Amrouch, Technische Universität München, Germany; Girish Pahwa, University of California, Berkeley; Yogesh Chauhan, IIT Kanpur, India

CRYOGENIC IN-MEMORY MATRIX-VECTOR MULTIPLICATION USING FERROELECTRIC SUPERCONDUCTING QUANTUM INTERFERENCE DEVICE (FE-SQUID)

Shamiul Alam, Jack Hutchins, Ahmedullah Aziz, University of Tennessee, Knoxville, TN; Md Shafayat Hossain, Princeton University, Princeton, NJ; Kai Ni, Rochester Institute of Technology, Rochester, NY; Vijaykrishnan Narayanan, Pennsylvania State University, University Park, PA

THERMAL SCAFFOLDING FOR ULTRA-DENSE 3D INTEGRATED CIRCUITS

Dennis Rich, Anna Kasperovich, Mohamadali Malakoutian, Robert Radway, Srabanti Chowdhury, Subhasish Mitra, Stanford University, Stanford, CA; Shiho Hagiwara, Takahide Yoshikawa, Fujitsu Research, Kawasaki, Japan

CORCPUM: EFFICIENT PROCESSING USING CROSS-POINT MEMORY VIA COOPERATIVE ROW-COLUMN ACCESS PIPELINING AND ADAPTIVE TIMING OPTIMIZATION IN SUBARRAYS

Chengning Wang, Dan Feng, Wei Tong, Jingning Liu, Huazhong University of Science and Technology, Wuhan, China

COMPACT AND HIGH-PERFORMANCE TCAM BASED ON SCALED DOUBLE-GATE FEFETS

Liu Liu, X. Sharon Hu, University of Notre Dame, South Bend, IN; Shubham Kumar, Simon Thomann, University of Stuttgart, Germany; Hussam Amrouch, Technische Universität München, Germany

FSD: A FAST SECURE DELETION STRATEGY FOR HIGH-DENSITY FLASH MEMORIES THROUGH WOM-V CODES

Jinhua Cui, Kai Tang, Laurence T. Yang, Huazhong University of Science and Technology, Wuhan, China

Research Sessions

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Panel

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PROGRAM

Wednesday, July 12, 2023

BOOSTING NEURAL NETWORKS THROUGH INNOVATIVE APPROXIMATION AND COMPRESSION

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Architecture Design

Room: 3010, 3rd Floor

Session Chair(s): Ganapati Bhat, Washington State University; Xiaoxiao Liu, AMD

Deep learning techniques have enjoyed ever-increasing accuracy and capabilities thanks to their massive tunable scaling parameters. However, this progress comes at the expense of computation, energy, and carbon footprint requirements. This session provides answers to a fundamental question. Do we have to perform every single operation to achieve the target performance? The papers will show innovative approaches to eliminate and approximate repetitive operations for dramatic efficiency gains with a minimal performance impact.

LIGHTNING TALK – HOW TO BOOST DEEP NEURAL NETWORKS FOR COMPUTER VISION

Soonhoi Ha, Seoul National University, Seoul, South Korea

FLEX-SFU: ACCELERATING DNN ACTIVATION FUNCTIONS BY NON-UNIFORM PIECEWISE APPROXIMATION

Enrico Reggiani, Renzo Andri, Lukas Cavigelli, Huawei, Zurich, Switzerland

A MEMORY-EFFICIENT EDGE INFERENCE ACCELERATOR WITH XOR-BASED MODEL COMPRESSION

Hyunseung Lee, Jihoon Hong, Soosung Kim, Seung Yul Lee, Jae W. Lee, Seoul National University, Seoul, South Korea

DYNAMIC SPARSE TRAINING VIA BALANCING THE EXPLORATION-EXPLOITATION TRADE-OFF

Shaoyi Huang, Hongwu Peng, Caiwen Ding, University of Connecticut, Storrs, CT; **Bowen Lei**, Texas A&M University, College Station, TX; **Dongkuan Xu**, North Carolina State University, Raleigh, NC; **Yue Sun**, Lehigh University, Bethlehem, PA; **Mimi Xie**, The University of Texas at San Antonio, TX

ALGORITHMS AND HARDWARE FOR EFFICIENT PROCESSING OF LOGIC-BASED NEURAL NETWORKS

Jingkai Hong, Arash Fayyazi, Amirhossein Esmaili, Mahdi Nazemi, Massoud Pedram, University of Southern California, Los Angeles, CA

HBP: HIERARCHICALLY BALANCED PRUNING AND ACCELERATOR CO-DESIGN FOR EFFICIENT DNN INFERENCE

Ao Ren, Jiaxing Shi, Duo Liu, Xianzhang Chen, Yujuan Tan, Chongqing University, Chongqing, China; **Yuhao Wang**, Meta, Menlo Park, CA; **Tao Zhang**, Rivos Inc., Mountain View, CA; **Yuan Xie**, University of California, Santa Barbara, CA

EFFICIENT NON-LINEAR ADDER FOR STOCHASTIC COMPUTING WITH APPROXIMATE SPATIAL-TEMPORAL SORTING NETWORK

Yixuan Hu, Tengyu Zhang, Meng Li, Renjie Wei, Yuan Wang, Runsheng Wang, Ru Huang, Peking University, Beijing, China; **Liangzhen Lai**, Meta, Sunnyvale, CA

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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DON'T CROSS ME! CROSS-LAYER SYSTEM SECURITY

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Embedded and Cross-Layer Security

Room: 3012, 3rd Floor

Session Chair(s): Farimah Farahmandi, University of Florida; Francesco Restuccia, University of California, San Diego
Security has permeated all aspects of system design – from application to architecture and down to the hardware. This session includes vulnerabilities and mitigations across the system stack, covering topics related to fault attacks, page table isolation, hardware memory management vulnerabilities, covert channels through synchronization primitives and thermal effect, and zero knowledge proof of ownership of a neural network.

LIGHTNING TALK – DON'T CROSS ME! CROSS-LAYER SYSTEM SECURITY

Houman Homayoun, University of California, Davis, CA

STALKER: A FRAMEWORK TO ANALYZE FRAGILITY OF CRYPTOGRAPHIC LIBRARIES UNDER HARDWARE FAULT MODELS

Guorui Xu, Fan Zhang, Xinjie Zhao, Yuan Chen, Shize Guo, Kui Ren, Zhejiang University, Hangzhou, China

PTSTORE: LIGHTWEIGHT ARCHITECTURAL SUPPORT FOR PAGE TABLE ISOLATION

Wende Tan, Yuan Li, Ying Liu, Jianping Wu, Chao Zhang, Tsinghua University, Beijing, China; Yangyu Chen, Chongqing University, Chongqing, China; **Yu Ding**, Google, San Jose, CA

LEAKY MDU: ARM MEMORY DISAMBIGUATION UNIT UNCOVERED AND VULNERABILITIES EXPOSED

Chang Liu, **Yongqiang Lyu**, Haixia Wang, Dapeng Ju, Dongsheng Wang, Tsinghua University, Beijing, China; Pengfei Qiu, Key Laboratory of Trustworthy Distributed Computing and Service (BUPT), Beijing, China; Gang Qu, Univ. of Maryland, College Park, MD

MES-ATTACKS: SOFTWARE-CONTROLLED COVERT CHANNELS BASED ON MUTUAL EXCLUSION AND SYNCHRONIZATION

Chaoqun Shen, **Jiliang Zhang**, Hunan University, Changsha, China; Gang Qu, Univ. of Maryland, College Park, MD

ZKROWN: ZERO KNOWLEDGE RIGHT OF OWNERSHIP FOR NEURAL NETWORKS

Nojan Sheybani, Ritvik Kapila, Farinaz Koushanfar, University of California, San Diego, CA; Zahra Ghodsi, Purdue University, Lafayette, IN

SMART DETECTION OF OBFUSCATED THERMAL COVERT CHANNEL ATTACKS IN MANY-CORE PROCESSORS

Jeferson Gonzalez-Gomez, Mohammed Bakr Sikal, Heba Khdr, Lars Bauer, Joerg Henkel, Karlsruhe Institute of Technology, Karlsruhe, Germany

EVERYTHING, EVERYPLACE, ALL AT ONCE!

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Physical Design and Verification

Room: 3002, 3rd Floor

Session Chair(s): Joseph Shinnerl, Siemens EDA; Jucemar Monteiro, Synopsys

This session presents advanced placement and floorplanning algorithms and MLCAD frameworks for modeling and parameter optimization. The first presentation leverages advances in optical flow prediction techniques for highly accurate congestion prediction. Next, GCN/GNN placement frameworks are deployed for congestion estimation and mitigation. A new wirelength model is born in the third presentation! The fourth work formulates an SDP to solve the floorplanning problem. This is followed by a GNN-based Steiner graph learning framework for sign-off quality timing prediction and optimization. The final paper presents an algorithm to efficiently solve the multi-height cell placement problem with minimum-implant-area and drain-to-drain abutment constraints.

LIGHTNING TALK – EVERYTHING, EVERYPLACE, ALL AT ONCE!

Andrew Kahng, University of California, San Diego, San Diego, CA

MITIGATING DISTRIBUTION SHIFT FOR CONGESTION OPTIMIZATION IN GLOBAL PLACEMENT

Su Zheng, Siting Liu, Bei Yu, Martin Wong, The Chinese University of Hong Kong, Hong Kong; Lancheng Zou, Wuhan University, Wuhan, China; Yibo Lin, Peking University, Beijing, China

PUFFER: A ROUTABILITY-DRIVEN PLACEMENT FRAMEWORK VIA CELL PADDING WITH MULTIPLE FEATURES AND STRATEGY EXPLORATION

Zhijie Cai, Peng Zou, Xingyu Tong, Jun Yu, Jianli Chen, Fudan University, Shanghai, China; Zhengtao Wu, Shanghai LEDA Technology Co., Ltd, Shanghai, China; Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

ON A MOREAU ENVELOPE WIRELENGTH MODEL FOR ANALYTICAL GLOBAL PLACEMENT

Peiyu Liao, Hongduo Liu, Bei Yu, Martin Wong, The Chinese University of Hong Kong, Hong Kong; Yibo Lin, Peking University, Beijing, China

GLOBAL FLOORPLANNING VIA SEMIDEFINITE PROGRAMMING

Wei Li, Jose Moura, Shawn Blanton, Carnegie Mellon University, Pittsburgh, PA; Fangzhou Wang, The Chinese University of Hong Kong, Hong Kong

MIXED-CELL-HEIGHT PLACEMENT WITH MINIMUM-IMPLANT-AREA AND DRAIN-TO-DRAIN ABUTMENT CONSTRAINTS

Guohao Chen, Benchao Zhu, Jiawei Li, Kun Wang, Jun Yu, Jianli Chen, Fudan University, Shanghai, China; Zheng Zeng, Fuzhou University, Fuzhou, China

CONCURRENT SIGN-OFF TIMING OPTIMIZATION VIA DEEP STEINER POINTS REFINEMENT

Siting Liu, Ziyi Wang, Bei Yu, Martin Wong, The Chinese University of Hong Kong, Hong Kong; Fangzhou Liu, Shanghai AI Laboratory, Shanghai, China; Yibo Lin, Peking University, Beijing, China

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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EXPANDING COMPUTE-IN-MEMORY FOR EMERGING MACHINE LEARNING

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): In-memory and Near-memory Computing Circuits and Architectures

Room: 3004, 3rd Floor

Session Chair(s): Cheng Wang, Iowa State University; Sumitha George, North Dakota State University

Deep learning technology is evolving quickly. Recent years have seen the emergence of new models and hardware-aware model architectures. This session helps push state of the art in this new direction by presenting new Compute-in-Memory (CIM) circuits and architectures for accelerating emerging attention models and collaborative hardware/neural architecture search for improving computation efficiency.

LIGHTNING TALK – IN-MEMORY COMPUTING FOR AI AND ML – A CROSS-LAYER PERSPECTIVE

Michael Niemier, University of Notre Dame, South Bend, IN

XPERT: PERIPHERAL CIRCUIT & NEURAL ARCHITECTURE CO-SEARCH FOR AREA AND ENERGY-EFFICIENT XBAR-BASED COMPUTING

Abhishek Moitra, Abhiroop Bhattacharjee, Youngeun Kim, Priyadarshini Panda, Yale University, New Haven, CT

TFIX: EXPLOITING THE NATURAL REDUNDANCY OF TERNARY NEURAL NETWORKS FOR FAULT TOLERANT IN-MEMORY VECTOR MATRIX MULTIPLICATION

Akul Malhotra, Chunguang Wang, Sumeet Gupta, Purdue University, West Lafayette, IN

MORPHABLE CIM: IMPROVING OPERATION INTENSITY AND DEPTHWISE CAPABILITY FOR SRAM-CIM ARCHITECTURE

Yun-Chen Lo, Ren-Shuo Liu, National Tsing Hua University, Hsinchu, Taiwan

IN-MEMORY NEURAL NETWORK ACCELERATOR BASED ON EDRAM CELL WITH ENHANCED RETENTION TIME

Inhwan Lee, Eunhwan Kim, Nameun Kang, Hyunmyung Oh, Pohang University of Science and Technology, Pohang, South Korea; Jae-Joon Kim, Seoul National University, Seoul, South Korea

RERAM-BASED GRAPH ATTENTION NETWORK WITH NODE-CENTRIC EDGE SEARCHING AND HAMMING SIMILARITY

Ruibin Mao, Can Li, The University of Hong Kong, Hong Kong; Xia Sheng, Catherine Graves, Cong Xu, Hewlett Packard Enterprise, Palo Alto, CA

ACCELERATING SPARSE ATTENTION WITH A RECONFIGURABLE NON-VOLATILE PROCESSING-IN-MEMORY ARCHITECTURE

Qilin Zheng, Shiyu Li, Yitu Wang, Ziru Li, Yiran Chen, Hai (Helen) Li, Duke University, Durham, NC

Research Sessions

Special Session

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TIMING-CRITICAL DESIGN AND ANALYSIS

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Time-Critical System Design

Room: 3008, 3rd Floor

Session Chair(s): Fanxin Kong, Syracuse University; Song Han, University of Connecticut

Timeliness is of particular importance for modern real-time embedded systems and applications. This session focuses on how to achieve and improve timeliness from different levels of hierarchy. The first presentation explores hardware acceleration of real time SoCs on RISC-V platforms. The second and third presentation investigate task allocation and scheduling on multiprocessor systems, while the fourth presentation looks into SRAM allocation and DNN task partitioning on edge TPUs. A novel analysis technique with data refreshing for reaction time to external events is shown in the fifth presentation. This session ends with a design space exploration of fault tolerance in timing sensitive networks with mixed-critical traffic.

LIGHTNING TALK – PROPERTY-BASED TIMING ANALYSIS AND OPTIMIZATION FOR COMPLEX CYBER-PHYSICAL REAL-TIME SYSTEMS

Tei-Wei Kuo, National Taiwan University, Taipei City, Taiwan

BLUEFACE: INTEGRATING AN ACCELERATOR INTO THE CORE’S PIPELINE THROUGH ALGORITHM-INTERFACE CO-DESIGN FOR REAL-TIME SOCS

Zhe Jiang, University of Cambridge, United Kingdom; **Nathan Fisher, Zheng Dong**, Wayne State University, Detroit, MI; **Nan Guan**, City University of Hong Kong, Hong Kong

HOLISTIC WCRT ANALYSIS FOR GLOBAL FIXED-PRIORITY PREEMPTIVE MULTIPROCESSOR SCHEDULING

Guoqi Xie, Chenglai Xiong, Wei Wu, Li Renfa, Hunan University, Hunan, China; **Wanli Chang**, University of York, United Kingdom

A UNIVERSAL METHOD FOR TASK ALLOCATION ON FP-FPS MULTIPROCESSOR SYSTEMS WITH SPIN LOCKS

Shuai Zhao, Sun Yat-Sen University, Guangzhou, China; **Nan Chen, Wanli Chang**, University of York, United Kingdom; **Yinjie Fang**, Hunan University, Changsha, China; **Zhao Li**, Shandong University of Technology, Zibo, China

SPET: TRANSPARENT SRAM ALLOCATION AND MODEL PARTITIONING FOR REAL-TIME DNN TASKS ON EDGE TPU

Changhun Han, Sangeun Oh, Ajou University, Suwon, South Korea; **Hoon Sung Chwa**, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; **Kilho Lee**, Soongsil University, Dongjak-gu, South Korea

REACTION TIME ANALYSIS OF EVENT-TRIGGERED PROCESSING CHAINS WITH DATA REFRESHING

Yue Tang, Xu Jiang, Wang Yi, Northeastern University, Shenyang, China; **Nan Guan**, City University of Hong Kong;; **Zheng Dong**, Wayne State University, Detroit, MI

FAULT TOLERANCE IN TIME-SENSITIVE NETWORKING WITH MIXED-CRITICAL TRAFFIC

Wenhong Ma, Xiangzhen Xiao, Guoqi Xie, Hunan University, Changsha, China; **Nan Guan**, City University of Hong Kong; **Yu Jiang**, Tsinghua University, Beijing, China; **Wanli Chang**, University of York, United Kingdom

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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TOWARDS WIDER ADOPTION OF NEAR-DATA PROCESSING

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): In-memory and Near-memory Computing

Architectures, Applications and Systems

Room: 3003, 3rd Floor

Session Chair(s): Xueqing Li, Tsinghua University; Jisung Park, POSTECH

Near-data processing (NDP) has been extensively investigated at almost all levels of the memory hierarchy as a promising paradigm that can overcome the fundamental limitations of von Neumann architecture. Even though a variety of NDP techniques have been proposed, there still exist multiple technical challenges that need to be addressed for a wide adoption of NDP solutions, such as NDP-aware compiler, data/resource allocation, and design space exploration. This session introduces four frameworks that aim to enable more efficient use of NDP solutions. In addition, two works for optimizing emerging memory/storage architecture are introduced.

LIGHTNING TALK – DEEP NEURAL NETWORK ACCELERATION USING RESISTIVE RAM BASED NEAR-MEMORY COMPUTING

Priyanka Raina, Stanford University, Stanford, CA

NMEXPLORER: AN EFFICIENT EXPLORATION FRAMEWORK FOR DIMM-BASED NEAR-MEMORY TENSOR REDUCTION

Cong Li, Zhe Zhou, Xingchen Li, Guangyu Sun, Peking University, Beijing, China; Dimin Niu, Alibaba Group, Sunnyvale, CA

PIMCOMP: A UNIVERSAL COMPILATION FRAMEWORK FOR CROSSBAR-BASED PIM DNN ACCELERATORS

Xiaotian Sun, Xinyu Wang, Wanqian Li, Lei Wang, Yinhe Han, Xiaoming Chen, University of Chinese Academy of Sciences, Beijing, China

BWA-NIMC: BUDGET-BASED WORKLOAD ALLOCATION FOR HYBRID NEAR/IN-MEMORY-COMPUTING

Chi-Tse Huang, Cheng-Yang Chang, Yu-Chuan Chuang, An-Yeu Wu, National Taiwan University, Taipei, Taiwan

RETHINKING PROGRAMMING FRAMEWORKS FOR IN-STORAGE PROCESSING

Yu-Chia Liu, **Kuan-Chieh Hsu**, Hung-Wei Tseng, University of California, Riverside, CA

ZONEKV: A SPACE-EFFICIENT KEY-VALUE STORE FOR ZNS SSDS

Mingchen Lu, Peiquan Jin, Xiaoliang Wang, Yongping Luo, University of Science and Technology of China, Hefei, China; Kuankuan Guo, ByteDance Inc., Beijing, China

HUNTER: RELEASING PERSISTENT MEMORY WRITE PERFORMANCE WITH A NOVEL PM-DRAM COLLABORATION ARCHITECTURE

Yanqi Pan, Yifeng Zhang, Wen Xia, Xiangyu Zou, Cai Deng, Harbin Institute of Technology, Shenzhen, Shenzhen, China

WHERE WILL AI CHANGE EDA: INSIDE, OUTSIDE OR NOT AT ALL?

Time: 3:30 PM – 5:30 PM

Event Type: Research Panel

Topic Area(s): AI, EDA

Room: 3014, 3rd Floor

Organizer(s): Andrew Kahng, University of California, San Diego, CA

Academic researchers, as well as the EDA industry and its major customers, have invested enormous effort and resources in the quest to apply AI in EDA and IC design. There is now a substantial body of production experience with AI-boosted EDA tools and design methodologies. Clearly, EDA can be helped by AI. For the DAC community, this motivates questions that seek a next level of understanding:

1. What benefits (from infusion of AI) have been seen by design organizations?
2. What areas/directions in EDA are now seen as “dead ends” for AI application?
3. What areas/directions are likely to bring the greatest future benefits?
4. Should we look for future benefits of AI “inside” vendor tools, or “outside” in customer deployment and methodology built around vendor tools?
5. Looking back from the year 2030, how will AI have fundamentally changed EDA and IC design?
6. Where do EDA suppliers and design organizations diverge the most in their envisioning of AI’s future in EDA and IC design?

This panel brings together experts from across tool development, business development, production deployment, and the leading edge of research for AI-boosted EDA. All panelists have deep experience with IC physical implementation and signoff, which has been a focus area for AI application in EDA.

Moderator: Leigh Anne Clevenger, Silicon Integration Initiative, Inc., Albany, NY

Panelists: Scot Weber, AMD, Austin, TX; Haoxing (Mark) Ren, NVIDIA, Austin, TX; Piyush Verma, Synopsys; Charles Alpert, Cadence Design Systems, Inc., Austin, TX; Paul Villarrubia, IBM, Austin, TX; Youngsoo Shin, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

THE DESIGN OF NEXT-GENERATION CLOUD COMPUTING SYSTEMS

Time: 3:30 PM – 5:30 PM

Event Type: Special Session (Research)

Topic Area(s): Cloud

Room: 3001, 3rd Floor

Organizer(s): Deming Chen, University of Illinois at Urbana-Champaign; Priya Nagpurkar, IBM

Cloud computing provides on-demand availability of computing resources for users. It allows enterprises to run their applications with improved manageability, less maintenance, and reduced overall cost. In addition, cloud computing is able to meet fluctuating computing demand through data/compute “bursting” across cloud boundaries. According to data reported by leading market analysis companies, the global spending on cloud computing services has reached \$706 billion now and expected to reach \$1.3 trillion by 2025. Important new cloud computing paradigms have emerged as well, including hybrid cloud and multi-cloud.

Designing efficient, performant, and secure cloud systems requires a holistic and systematic approach and novel interdisciplinary research. This is due to the unique challenges faced by future clouds: high system complexity, difficulty for test, evaluation, and monitoring, vulnerability from security attacks and data leakage, unpredictable latency, non-ideal system configurations, high energy and carbon emission, and complicated communicating interfaces across multi-clouds. Each of these challenges, if not solved well, will become a roadblock for the future growth and promises of cloud computing.

In this special session, four prominent industrial leaders with excellent cloud computing expertise from large cloud or computing hardware vendors will share their unique insights, vision, and solutions for the design of the next-generation cloud computing systems. They will focus on grand future opportunities, challenges, and promising research solutions and directions. The special session will provide a holistic and interdisciplinary coverage for the design of the next-generation cloud computing systems in areas including application and algorithm design, AI for system design, distributed computing, big-data storage, cloud computing infrastructure, computer architecture and accelerator design, security and privacy, and design automation across different system stacks.

AI SOFTWARE IS LEADING THE HARDWARE DEVELOPMENT IN CLOUD COMPUTING

Ivo Bolsens, AMD, San Jose, CA

IF YOU BUILD IT, WILL THEY COME? OVERCOMING DEPLOYMENT CHALLENGES OF CUSTOM HARDWARE ACCELERATORS IN THE CLOUD

Andrew Putnam, Microsoft, Redmond, WA

ARCHITECTING PRODUCTS FOR THE CLOUD

Annie Foong, Intel

ARCHITECTURE AND SOFTWARE STACK FOR THE NEXT-GENERATION CLOUD COMPUTING SYSTEMS

Wen-mei Hwu, University of Illinois at Urbana-Champaign, IL

ENGINEERING THE FUTURE OF CLOUD SOFTWARE WITH AI

Ruchir Puri, IBM, Yorktown Heights, NY

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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WEDNESDAY ENGINEERING TRACK POSTER RECEPTION

Time: 5:00 PM – 6:00 PM

Event Type: Engineering Track Poster

Room: Level 2 Exhibit Hall

3D IC INTER-DIE TEST IMPLEMENTATION USING IEEE1838

Keunsoo Lee, Kunhyuk Kang, Samsung Electronics, Hwaseong, South Korea; Joon Kim, Synopsys, Seongnam-si, South Korea; Vistrita Tyagi, Synopsys, Bangalore, India

3DIC DESIGN FLOORPLANNING FLOW AND EARLY AREA ESTIMATION FOR AREA OPTIMIZATION

Yongjin Hong, Jongho Kim, Jun Seomun, Sangyun Kim, Samsung Electronics, Hwaseong, South Korea

A DATA ANALYTICS BASED APPROACH FOR REDUCING CLOCK TREE POWER AT RTL

Manish Kumar, Vishnu Kanwar, Vishal Kashyap, Gaurav Garkoti, Mohammed Fahad, Amit Dey, Siemens EDA, Noida, India; Divya Bareja, Bhupesh Prajapat, Vijay Tayal, Siemens EDA, Delhi, India

A MACHINE LEARNING APPROACH TOWARDS SKILL CODE AUTOCOMPLETION

Enrique Dehaerne, KU Leuven, Belgium;

A NOVEL HIERARCHICAL POWER INTEGRITY SIGNOFF METHODOLOGY FOR ULTRA LARGE SOCS

Rossana Liu, Microsoft, Austin, TX; Medha Kulkarni, Microsoft, Mountain View, CA; Pranav Ranganathan, Microsoft, Raleigh, NC; Piyush Jain, Microsoft, Hillsboro, OR; Rushin Patel, Cadence Design Systems, Inc., San Francisco, CA; Ajit Gokhale, Cadence Design Systems, Inc., Cary, NC; Lucas Chaves, Cadence Design Systems, Inc., Belo Horizonte, Brazil

ACCELERATING DATAPATH VERIFICATION USING FORMAL TECHNIQUES

Bhavya Sri Dasari, Karthik Rajakumar, Texas Instruments, Bangalore, India; Jaaneshwaran A, Texas Instruments, Chennai, India; Craig Deaton, Cadence Design Systems, Inc., Austin, TX; Uday Kumar, NIT Warangal, Hyderabad, India

ADVANCED NODE PPA AND DESIGN OPTIMIZATION USING CEREBRUS ML FLOW

Rahul Mandal, Balamurugan Sekar, Kiran Kumar, Marvell, Bangalore, India; Samuel Di Pietro, Marvell, Boston, MA

AN ACCURATE SYSTEM LEVEL TRANSIENT VOLTAGE DROOP ANALYSIS METHODOLOGY FOR HIGH PERFORMANCE GPGPU POWER DELIVERY NETWORK

Yuanyuan Ling, Ling Sun, Tieqing Chen, Zhenhua Gan, Shixuan Que, Shuqiang Zhang, Xiaoxia Zhou, Iluvatar, Shanghai, China

AN EFFICIENT AND SPICE ALIGNED METHOD FOR COMPLEX IO'S BEHAVIORAL MODEL GENERATION AND VERIFICATION

Natish Singla, Saurabh Srivastava, Harsh Garg, Avinav Joshi, Atul Bhargava, STMicroelectronics, Noida, India; Matthieu Fillaud, Siemens EDA, Grenoble, France; Anil Dwivedi, STMicroelectronics, Delhi, India

AN EFFICIENT METHODOLOGY TO VERIFY FLOATING POINT MATRIX MULTIPLICATION

Nicolae Tusinschi, Siemens EDA, Munich, Germany; Gerardo Nahum, Siemens EDA, Haifa, Israel; Sasa Stamenkovic, Siemens EDA, San Jose, CA

AUTOMATED ANALOG MODEL GENERATION FOR HIGH QUALITY VERIFICATION USING EVENT DRIVEN SIMULATORS

Aadhar Sharma, Lakshmanan Balasubramanian, Saurabh Pandey, Texas Instruments (India) Pvt. Ltd., Bangalore, India; Aastha Nitesh Dave, Technische Universität München, Germany; Mayank Mehta, Lg Ad Solutions, Faridabad, India; Jaeha Kim, Seoul National University, Seoul, South Korea

AUTOMATIC GENERATION OF 22FDX® OPAMP DESIGNS IN THE VIRTUOSO® SUITE BY INCORPORATING ID-XPLORE™ FOR SIZING WITH IIP LAYOUT GENERATORS

Benjamin Prautsch, Fraunhofer IIS/EAS, Dresden, Germany; Ramy Iskander, Intento Design, Paris, France

AUTOMATED AND INTEGRATED DYNAMIC VOLTAGE DROP IR-ECO FLOW ON AUTOMOTIVE ADAS SOCS

Manish Kumar, Govind Pal, Samant Paul, Anil Yadav, Atul Bhargava, STMicroelectronics, Noida, India; Amit Jangra, Ansys, Uttar Pradesh, India; Koshy John, Ansys, San Jose, C

BRIDGING IR DROP AND TIMING ANALYSIS SIGNOFF FOR EXECUTION EXCELLENCE IN GRAPHICS DESIGNS

Srim Karthik Kanneganti, Intel, Sacramento, CA

CHALLENGES AND CUSTOM METHODOLOGY INVOLVED IN SUCCESSFUL PHYSICAL IMPLEMENTATION OF C-SHAPED / WRAPPED DDRPHY IP SOLUTION

Sachin Revannavar, Saiprasad Gollapinni, Pushpanjali Pinnu, Roshan Kumar, Gangadhar Naik, Marvell Semiconductor, Bangalore, India; Greg Ford, Marvell Semiconductor, Santa Clara, C

CHIPLET DESIGN AND VERIFICATION USING AN OPEN STANDARD MARKUP LANGUAGE

James Wong, Jawad Nasrullah, Palo Alto Electron, San Francisco, CA

CLUSTERING OF ASSERTIONS USING ML/AI IN FORMAL VERIFICATION

Viraj Rawal, Synopsys, Noida, India; S R Pavitra, Synopsys, Gwalior, India; Vishwajith Rao, Synopsys, Bangalore, India

EFFICIENT METHODOLOGIES FOR STL CERTIFICATION OF SPINOFF SOC DESIGNS.

Arif Mohammed, Chandra Has Dondapati, Sanjay Singh, Vishal Bhadauria, Subham Mohapatra, Prasanth Viswanathan Pillai, Texas Instruments, Bangalore, India; Krishna Allam, Texas Instruments, Houston, TX

ELECTRICAL ANALYSIS USING HIERARCHICAL APPROACH ON ULTRA LARGE DESIGNS

Sainarayanan Karatholuvu Suryanarayanan, Rakesh Thadimarri Reddy, Marvell, Bangalore, India

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WEDNESDAY ENGINEERING TRACK POSTER RECEPTION (CONTINUED)

EM/IR SIGNOFF METHODOLOGY FOR LARGE SIZE MIXED SIGNAL CUSTOM BLOCKS IN HIGH SPEED IOS

Ayan Roy Chowdhury, Intel, Karnataka, India; Richa Agrawal, Intel, Warangal, India

FORMAL VERIFICATION CONTRACT BASED SOC SECURITY VALIDATION

Kiran Rampurkar, Ketan Baladaniya, Harshal Mumbaikar, Manoj Kumar Munigala, Surinder Sood, Intel, Karnataka, India;

HAZARD DETECTION TOOL IN ASYNCHRONOUS FINITE STATE MACHINES TRANSITION LOGIC

Roberta Priolo, Francesco Battini, Enea Dimroci, STMicroelectronics, Milano, Italy

HIGH-PERFORMANCE DESIGN WITH RAPID RTL PROFILING OF CRITICAL POWER SCENARIOS

Alexander Pivovarov, Mehdi Sadi, AMD, Toronto, Canada; Vidhu Joshi, AMD, Bangalore, India

HW SECURITY PATH VALIDATION USING FORMAL METHODS: INTEL CASE STUDIES

Alex Levin, Intel, Tel Aviv, Israel; Sayak Ray, Intel, San Jose, CA

IMPROVING DESIGN ROBUSTNESS BY ACCOUNTING FOR DEVICE SKEW IN STATIC TIMING ANALYSIS

Aftab Khan, Synopsys, Taipei, Taiwan; Wenwen Chai, Synopsys, San Francisco, CA; Ayhan Mutlu, Synopsys, Los Gatos, CA; Li Ding, Synopsys, San Jose, CA

INTEGRATION OF INTEL THERMAL MODEL WITH DESIGN-FOR-RELIABILITY FLOW

Lei Jiang, Intel, Camas, WA; Daniel Pantuso, Mike Wang, Intel, Portland, OR; Prabhakar Marepalli, Colin Landon, Mohammed Shahid, Intel, Hillsboro, OR; Sanjay Murthy, Intel, Phoenix, AZ

INTENT BASED TIMING CONSTRAINTS

Hemlata Gupta, Kerim Kalafala, IBM, Hopewell Junction, NY; Adil Bhanji, IBM, Wappinger Falls, NY; Manish Verma, IBM, Bangalore, India; Jennifer Basile, IBM, Poughkeepsie, NY; Jack DiLullo, IBM, Austin, TX

IO DESIGNS FOR RELIABILITY IN ADVANCED TECHNOLOGY NODES

Manoj Kumar, Kailash Kumar, Akhil Thotli, Prateek Singh, Nitin Bansal, Synopsys, Noida, India

LEVERAGING INTEGRATED SILICON PHOTONICS FOR A STREAMLINED GPU ARCHITECTURE

Luca Ramini, Jinsung Youn, Marco Fiorentino, Steven Dean, Raymond Beausoleil, Hewlett Packard Enterprise, Palo Alto, CA

NOVEL CAD METHODOLOGY FOR IR DROP AND RELIABILITY VERIFICATION OF STACKED DIES (3D-IC)

Matthew Jastrzebski, Roger Hayward, Intel, Beaverton, OR; Noel Pereira, Intel, Santa Clara, CA

NOVEL CHIP-PACKAGE-SYSTEM THERMAL ANALYSIS WITH RTL POWER

Chenyang Zhang, Chen Lin, Bin Guo, Sanechips Technology Co., Ltd, Shenzhen, China; Zhongming Hou, Shuqiang Zhang, Ansys, Shanghai, China

NOVEL HIERARCHICAL IREM SIGN-OFF FLOW USING ROM

Dongyoun Yi, Seonghun Jeong, Byunghyun Lee, Samsung Electronics, Hwaseong, South Korea

OVERCOMING CHALLENGES IN FUNCTIONAL VERIFICATION OF AUTOMOTIVE TRAFFIC SCHEDULERS

Harshit Jaiswal, Cadence Design Systems, Inc., Bangalore, India; Hemlata Bist, Cadence Design Systems, Inc., Noida, India

REUSE OF LINT WAIVERS: AN APPROACH TO RELAY KNOWLEDGE & GUIDE SYNTHESIS

Amit Goldie, Himanshu Kathuria, Synopsys, Noida, India; Suresh Barla, Synopsys, San Jose, CA; Vrinda Padmakumari, Synopsys, Sunnyvale, CA

RV (RELIABILITY VERIFICATION) AUTOMATION TO IMPROVE EXECUTION EFFICIENCY

Raj Dua, Intel, Santa Clara, CA; Brahmaiah Throvagunta, Narendra Kumar Bhuma, Priyanka Bhagwat, Sandeep Dappilli, Intel, Bangalore, India

SIGMADVD (SDVD): HIGH COVERAGE SOLUTION FOR POWER INTEGRITY SIGNOFF

Anusha Vemuri, Emmanuel Chao, NVIDIA, San Francisco, CA; Santosh Santosh, NVIDIA, Santa Clara, CA; Chidambaram Rakkappan, Ansys, Vancouver, Canada; Ed Deeters, Ansys, Austin, TX

SPECIAL BIT PATTERN INJECTION IN SIMULATION VERIFICATION BY LEVERAGING FORMAL VERIFICATION

Viraj Rawal, Vishwajith Rao, Nivin George, Synopsys, Bangalore, India

STATIC ANALYSIS FOR EARLY DETECTION AND EFFICIENT DEBUG

Hormoz Yaghtiel, Alif Semiconductor, San Jose, CA; Guru Shindaghatta, Real Intent Inc, Aliso Viejo, CA; Kanad Chakraborty, Real Intent Inc, Portland, OR

TIPS & FACTS THAT EVERY DESIGN ENGINEER SHOULD KNOW ABOUT RTL SYNTHESIS

Clifford Cummings, Paradigm Works, Inc., Provo, UT

Research Sessions

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Engineering Track

LATE BREAKING RESULTS POSTER RECEPTION

Time: 6:00 PM – 7:00 PM

Event Type: Late Breaking Results Poster

Room: Level 2 Lobby

LATE BREAKING RESULTS: AN EFFICIENT BRIDGE-BASED COMPRESSION ALGORITHM FOR TOPOLOGICALLY QUANTUM ERROR CORRECTED CIRCUITS

Wei-Hsiang Tseng, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

LATE BREAKING RESULTS: ANALYTICAL PLACEMENT FOR 3D ICs WITH MULTIPLE MANUFACTURING TECHNOLOGIES

Yan-Jen Chen, Yan-Syuan Chen, Wei-Che Tseng, Cheng-Yu Chiang, Yu-Hsiang Lo, Yao-Wen Chang, National Taiwan University, Taipei, Taiwan

LATE BREAKING RESULTS: CONFIGURABLE RING OSCILLATORS AS A SIDE-CHANNEL COUNTERMEASURE

Hassan Nassar, Simon Pankner, Lars Bauer, Joerg Henkel, Karlsruhe Institute of Technology, Karlsruhe, Germany

LATE BREAKING RESULTS: COPPER: COMPUTATION OBFUSCATION BY PRODUCING PERMUTATIONS FOR ENCODING RANDOMLY

Kevin Hutto, Vincent Mooney, Georgia Institute of Technology, Atlanta, GA

LATE BREAKING RESULTS: FAST FAIR MEDICAL APPLICATIONS? HYBRID VISION MODELS ACHIEVE THE FAIRNESS ON THE EDGE

Changdi Yang, Peiyan Dong, Zhenglun Kong, Yanyu Li, Pinrui Yu, Northeastern University, Boston, MA; Yi Sheng, Lei Yang, George Mason University, Fairfax, VA

LATE BREAKING RESULTS: FROM HYBRID DESIGN AUTOMATION FOR FIELD-COUPLED NANOTECHNOLOGIES

Simon Toni Hofmann, Marcel Walter, Lorenzo Servadei, Robert Wille, Technische Universität München, Germany

LATE BREAKING RESULTS: PIE-DRAM: POSTPONING IECC TO ENHANCE DRAM PERFORMANCE WITH ACCESS TABLE

JaeHwa Jeon, Jae-Youn Hong, Sunghoon Kim, Insu Choi, Joon-Sung Yang, Yonsei University, Seoul, South Korea

LATE BREAKING RESULTS: PVC-RAM: PROCESS VARIATION AWARE CHARGE DOMAIN IN-MEMORY COMPUTING 6T-SRAM FOR DNNS

Sai Shubham, Shubham Bhagavandas, Kailash Prasad, Joyce Meki, Indian Institute of Technology, Gandhinagar, India

LATE BREAKING RESULTS: PVT-SENSITIVE DELAY FITTING FOR HIGH PERFORMANCE COMPUTING

Ding-Hao Wang, Pei-Ju Lin, Hui-Ting Yang, Global UniChip Corp., Hsinchu, Taiwan; Shuo-Hung Hsu, Hsu-Shiang Yang, Mark Po-Hung Lin, National Yang Ming Chiao Tung University, Tainan, Taiwan

LATE BREAKING RESULTS: PYAIE: A PYTHON-BASED PROGRAMMING FRAMEWORK FOR VERSAL ACAP PLATFORMS

Hongzheng Tian, Shining Yang, Yoonha Cha, Sitao Huang, University of California, Irvine, CA

LATE BREAKING RESULTS: RL-LPO: REINFORCEMENT LEARNING BASED LEAKAGE POWER OPTIMIZATION FRAMEWORK WITH GRAPH NEURAL NETWORK

Jiahao Wang, Peng Cao, Southeast University, Jiangsu, China

LATE BREAKING RESULTS: RQ-DNN: RELIABLE QUANTIZATION FOR FAULT-TOLERANT DEEP NEURAL NETWORK

Insu Choi, Jae-Youn Hong, JaeHwa Jeon, Joon-Sung Yang, Yonsei University, Seoul, South Korea

LATE BREAKING RESULTS: SCALABLE AND EFFICIENT HYPERDIMENSIONAL COMPUTING FOR NETWORK INTRUSION DETECTION

Junyao Wang, Hanning Chen, Mariam Issa, Sitao Huang, Mohsen Imani, University of California, Irvine, CA

LATE BREAKING RESULTS: TEST SELECTION FOR RTL COVERAGE BY UNSUPERVISED LEARNING FROM FAST FUNCTIONAL SIMULATION

Rongjian Liang, NVIDIA, College Station, TX; Nathaniel Pinckney, Haoxing Ren, Brucek Khailany, NVIDIA, Austin, TX; Yuji Chai, Harvard University, Cambridge, MA

LATE BREAKING RESULTS: WEIGHT DECAY IS ALL YOU NEED FOR NEURAL NETWORK SPARSIFICATION

Xizi Chen, Rui Pan, Huazhong Agricultural University, Huazhong, China; Xiaomeng Wang, Fengshi Tian, Chi-Ying Tsui, Hong Kong University of Science and Technology, Hong Kong

Research Sessions

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Engineering Track

NETWORKING RECEPTION & WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 PM – 7:00 PM

Event Type: Work-in-Progress Poster

Room: Level 2 Lobby

A DEEP LEARNING FRAMEWORK FOR VERILOG AUTOCOMPLETION TOWARDS DESIGN AND VERIFICATION AUTOMATION

Enrique Dehaerne, Stefan De Gendt, KU Leuven, Belgium; Bappaditya Dey, Sandip Halder, imec, Leuven, Belgium

A HIGHLY EFFICIENT REINFORCEMENT LEARNING BASED DFG MAPPING METHOD ON CGRA

Tanvir Ahmed, Yuko Hara-Azumi, Tokyo Institute of Technology, Tokyo, Japan

A RISC-V INSTRUCTION LEVEL ACCELERATION FOR FFT

Shijie Jiang, Yi Zou, Wanwan Li, South China University of Technology, Guangzhou, China; Hao Wang, University of Science and Technology of China, Hefei, China

A TRANSFER LEARNING FRAMEWORK FOR HIGH-ACCURATE CROSS-WORKLOAD DESIGN SPACE EXPLORATION OF CPU

Duo Wang, Mingyu Yan, Haoran Dang, Xin Liu, Yihan Teng, Wenming Li, Xiaochun Ye, Dongrui Fan, University of Chinese Academy of Sciences, Beijing, China

A UNIFYING TENSOR VIEW FOR LIGHTWEIGHT CNNs

Jason Chun Lok Li, Rui Lin, Jiajun Zhou, Edmund Yin Mun Lam, Ngai Wong, The University of Hong Kong, Hong Kong

ACCELERATING IRREGULAR APPLICATIONS ON DATAFLOW ARCHITECTURES THROUGH SOFTWARE AND HARDWARE CO-DESIGN

Zhihua Fan, Wenming Li, Shengzhong Tang, Xuejun An, Xiaochun Ye, Dongrui Fan, Institute of Computing Technology, Beijing, China

ACCURATE AND FAST METHOD TO CLOSE DESIGN VS SILICON GAP

Moonsu Kim, Changho Han, Jaeyoung Lim, Sunik Heo, Jaehyeon Kang, Cheoljun Bae, Hyundon Kim, Hyunseung Seo, Kunhyuk Kang, Sungung Kwak, Sangyun Kim, Samsung Electronics, Hwaseong, South Korea; Li Ding, Synopsys, San Jose, CA; Asheesh Baghel, Synopsys, Hwaseong, India; Ruijing Shen, Synopsys, New York City, NY

APEX: RECOMMENDING DESIGN FLOW PARAMETERS USING A VARIATIONAL AUTOENCODER

Michael Kazda, IBM, Poughkeepsie, NY; George Antony, IBM, Bengaluru, India; Michael Monkowski, IBM, East Fishkill, NY

APPLYING GRAPH EXPLANATION TO OPERATOR FUSION

Keith Mills, Muhammad Qharabagh, Weichen Qiu, University of Alberta, Edmonton, Canada; Fred Han, Mohammad Salameh, Wei Lu, Huawei, Edmonton, Canada

ARROW: A SOFT RISC-V VECTOR ACCELERATOR FOR MACHINE LEARNING INFERENCE

Imad Al Assir, Mohamad El Iskandarani, Hadi Al Sandid, Mazen Saghir, American University of Beirut, Lebanon

AUTOMATED FEEDTHROUGH PATH GENERATION AND VALIDATION FLOW AT RTL LEVEL BASED ON FLOORPLAN AWARE SPECIFICATION OF CHANNEL-LESS SOC

Bhrugurajsinh Chudasama, Intel, Palo Alto, CA; Vinay Kumar, Intel, Bangalore, India; Wilson Chan, Intel, Fremont, CA

CASCADE: AN APPLICATION PIPELINING TOOLKIT FOR COARSE-GRAINED RECONFIGURABLE ARRAYS

Jackson Melchert, Yuchen Mei, Qiaoyi Liu, Kalhan Koul, Mark Horowitz, Priyanka Raina, Stanford University, Stanford, CA

CLASSIFICATION PREDICTION ATTACK OVER SPARSITY-AWARE EMBEDDED NEURAL NETWORKS USING TIMING-BASED SIDE-CHANNEL LEAKAGE

Saurav Maji, Kyungmi Lee, Anantha Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA

CLUSTER-BASED HIERARCHICAL HLS DESIGN OPTIMIZATION

Aggelos Ferikoglou, Andreas Kakolyris, Vasilis Kakolyris, Dimosthenis Masouros, Dimitrios Soudris, National Technical University of Athens, Greece; Sotirios Xydis, Harokopio University of Athens, Athens, Greece

COMPREHENSIVE ANALYSIS OF HYPERDIMENSIONAL COMPUTING AGAINST GRADIENT-BASED ATTACKS

Hamza Errahmouni Barkam, SungHeon Jeong, Zhuowen Zou, Calvin Yeung, Mohsen Imani, University of California, Irvine, CA; Sanggeon Yun, Kookmin University, Seoul, South Korea; Xun Jiao, Villanova University, Villanova, PA

CONTEXT-AWARE RUNTIME MODEL RECONFIGURATION FOR ENERGY-EFFICIENT AUTONOMOUS VEHICLE PERCEPTION

Yifan Zhang, Arnav Malawade, Xiaofang Zhang, Mohammad Al Faruque, Sitao Huang, University of California, Irvine, CA

CR2: A COMPRESSED RERAM-BASED DNN ACCELERATOR BY COMBINING COMPUTATION AND READ OPERATION

Shi-Hao Hong, Yeh-Ching Chung, The Chinese University of Hong Kong, Shenzhen, China

DAG-AWARE SYNTHESIS ORCHESTRATION

Yingjie Li, Mingju Liu, Cunxi Yu, University of Utah, Salt Lake City, UT; Alan Mishchenko, University of California, Berkeley, CA

DEMANDS FOR OPEN-SOURCE HARDWARE TROJAN DETECTION TOOLS: AN RL APPROACH

Amin Sarihi, Abdel-Hameed A. Badawy, New Mexico State University, Las Cruces, NM; Peter Jamieson, Miami University, Oxford, OH; Ahmad Patooghy, North Carolina Agricultural and Technical State University, Greensboro, NC

EFFICIENT TRANSFORMATION OF ARCHITECTURES THROUGH HARDWARE-AWARE NONLINEAR OPTIMIZATION

Zhen Dong, Kurt Keutzer, University of California, Berkeley, CA; Hongxu Yin, Arash Vahdat, Jan Kautz, Pavlo Molchanov, NVIDIA, San Jose, CA

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NETWORKING RECEPTION & WORK-IN-PROGRESS POSTER SESSION (CONTINUED)

ENERGY-EFFICIENT PERSONALIZED FEDERATED SEARCH WITH GRAPH FOR EDGE COMPUTING

Zhao Yang, Qingshuang Sun, Northwestern Polytechnical University, Xi'an, China

EPHA: AN ENERGY-EFFICIENT PARALLEL HYBRID ARCHITECTURE FOR AGI VIA NEUROMORPHIC COMPENSATED FERRIMAGNETS

Yun Zhao, Sheng Ma, Liang Fang, Li Huang, National University of Defense Technology, ChangSha, China

FORNAX: LIGHTWEIGHT ENERGY-EFFICIENT DNN ACCELERATOR ARCHITECTURE FOR EDGE DEVICES

Chanho Park, Semin Koong, Bogil Kim, Taesoo Lim, William Song, Yonsei University, Seoul, South Korea

FPGA IMPLEMENTATION OF EFFICIENT 2D-FFT BEAMFORMING FOR ON-BOARD PROCESSING IN SATELLITES

Rakesh Palisetty, Geoffrey Eappen, Vibhum Singh, Luis Garces Socarras, Vu Ha, Juan Peralvo, Joerge, Rios, Juan Merlano Duncan, Wallace Martins, Symeon Chatzinatos, Bjorn Ottersten, University of Luxembourg, Luxembourg; Bingen Cortazar, Salvatore D'Addio, Piero Angeletti, European Space Agency, Keplerlaan, Netherlands

FROM STATIC ANALYSES TO RUNTIME VERIFICATION OF CYBER-PHYSICAL SYSTEMS

Guillaume Roumage, University Paris-Saclay, Saclay, France; Selma Azaiez, CEA, LIST, Saclay, France; Stephane Louise, University Paris-Saclay, Gif-sur-Yvette, France

FURRY: ACCELERATING DEPTHWISE CONVOLUTIONS ON SYSTOLIC ARRAYS USING FLATTENED CONVOLUTION WINDOWS

Mingeon Park, Seokjin Hwang, Hyungmin Cho, Sungkyunkwan University, Suwon, South Korea

FUSED M: ACCELERATING DIFFUSION MODEL SAMPLING ON VERSAL ACAP ARCHITECTURE

Tuo Dai, Bizhao Shi, Guojie Luo, Peking University, Beijing, China

GCN-BASED FLOORPLANNING WITH DIRICHLET BOUNDARY CONDITIONS

Yiting Liu, Mingzhi Dong, Ziyi Ju, Fan Yang, Xuan Zeng, Li Shang, Fudan University, Shanghai, China; Hai Zhou, Northwestern University, Evanston, IL; Jia Wang, Illinois Institute of Technology, Chicago, IL

GEBA: GRADIENT-ERROR-BASED APPROXIMATION OF ACTIVATION FUNCTIONS

ChangMin Ye, Doo Seok Jeong, Hanyang University, Seongdong-gu, South Korea

HIGH-DENSITY DIGITAL NEUROMORPHIC PROCESSOR WITH HIGH-PRECISION NEURAL AND SYNAPTIC DYNAMICS

Jongkil Park, YeonJoo Jeong, Jaewook Kim, Suyoun Lee, Joon Young Kwak, Jong-keuk Park, Inho Kim, KIST, Seoul, South Korea

IMPROVING TIMING ERROR PREDICTION VIA MICROARCHITECTURE-AWARE STOCHASTIC SEARCH AND MACHINE LEARNING

Styliani Tompazi, Ioannis Tsiokanos, Lev Mukhanov, Jesus Martinez del Rincon, Queen's University Belfast, United Kingdom

LATENCY-BOUNDED CLOCK MESH SYNTHESIS METHODOLOGY BASED ON DYNAMIC PROGRAMMING

Meng Liu, Beijing University of Technology, Beijing, China

LEVERAGING THE RESIDUE NUMBER SYSTEM FOR DESIGNING HIGH-PRECISION ANALOG DEEP NEURAL NETWORK ACCELERATORS

Cansu Demirkiran, Rashmi Agrawal, Ajay Joshi, Boston University, Boston, MA; Vijay Janapa Reddi, Harvard University, Cambridge, MA; Darius Bunandar, Lightmatter, Boston, MA

MACHINE LEARNING BASED DESIGN METHODOLOGY FOR POWER OPTIMIZATION OF WIDE RANGE SRAM

Junseo Lee, Jihwan Park, Inseong Jeon, Hanwool Jeong, Kwangwoon University, Seoul, South Korea

MALICE: MANIPULATION ATTACKS ON LEARNED IMAGE COMPRESSION

Kang Liu, Di Wu, Yangyu Wu, Dan Feng, Huazhong University of Science and Technology, Wuhan, China; Yiru Wang, Beijing University of Posts and Telecommunications, Beijing, China; Benjamin Tan, University of Calgary, Canada; Siddharth Garg, New York University, Brooklyn, NY

MCTHSL: 4x4-DEVICE-MATRIX-BASED COST-OPTIMIZED TNU-RECOVERY HIS-INSENSITIVE AND SET-FILTERABLE LATCH FOR AEROSPACE APPLICATIONS

Aibin Yan, Zhuoyuan Lin, Jie Cui, Anhui University, Hefei, China; Zhengfeng Huang, Hefei University of Technology, Hefei, China; Tianming Ni, Anhui Polytechnic University, Wuhu, China; Patrick Girard, LIRMM / CNRS, Montpellier, France; Xiaoqing Wen, Kyushu Institute of Technology, Fukuoka, Japan

MICRONAS: ZERO-SHOT NEURAL ARCHITECTURE SEARCH FOR MCUS

Ye Qiao, Haocheng Xu, Yifan Zhang, Sitao Huang, University of California, Irvine, CA

MOVE-ON-COVER: AN EFFICIENT SECURE DELETION STRATEGY FOR INTERLACED MAGNETIC RECORDING

Zhimin Zeng, Jinhua Cui, Lizhao Wan, Laurence T. Yang, Huazhong University of Science and Technology, Wuhan, China

MULTI-OBJECTIVE OPTIMIZATION FOR FLOATING POINT MIX-PRECISION TUNING

Zeqing Li, Youhui Zhang, Tsinghua University, Beijing, China

NEAR-MEMORY COMPUTING WITH COMPRESSED EMBEDDING TABLE FOR PERSONALIZED RECOMMENDATION

Jeongmin Lim, Kyungpook National University, Daegu, South Korea; Young Geun Kim, Sung Woo Chung, Korea University, Seoul, South Korea; Farinaz Koushanfar, University of California, San Diego, CA; Joonho Kong, Kyungpook National University, Daegu, South Korea

Research Sessions

Special Session

Panel

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Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

NETWORKING RECEPTION & WORK-IN-PROGRESS POSTER SESSION (CONTINUED)

NEURO-PDR: INTEGRATING NEURAL NETWORKS IN PDR ALGORITHM FOR HARDWARE MODEL CHECKING

Guangyu Hu, Hongce Zhang, Wei Zhang, Hong Kong University of Science and Technology, Hong Kong

NONL-DFR: NEW MODEL OF DIGITAL DELAYED FEEDBACK RESERVOIR WITHOUT NONLINEAR ELEMENTS

Sosei Ikeda, Hiromitsu Awano, Takashi Sato, Kyoto University, Kyoto, Japan

NOVEL ADAPTIVE QUANTIZATION METHODOLOGY FOR 8-BIT FLOATING-POINT DNN TRAINING

Mohammad Hassani Sadi, Technische Universität Kaiserslautern, Germany; Chirag Sudarshan, Norbert Wehn, University of Kaiserslautern, Germany

OASR-WFBP: AN OVERLAPPING AWARE STARTUP SHARING GRADIENT MERGING STRATEGY FOR EFFICIENT COMMUNICATION IN DISTRIBUTED DEEP LEARNING

Yingjie Song, Zhuo Tang, Zhizhong Liu, Ruixing Zong, Kenli Li, Hunan University, Changsha, China; Yaohua Wang, National University of Defense Technology, Changsha, China; Xiantao Zhang, Alibaba Group, Hangzhou, China

PROHASH: A PROMOTION-BASED HASHING INDEX SCHEME FOR NVM-BASED SYSTEMS

Bo-Jun Chen, Wei-Kuan Shih, National Tsing Hua University, Hsinchu, Taiwan; Yen-Ting Chen, Yuan-Hao Chang, Academia Sinica, Taipei, Taiwan; Yu-Pei Liang, National Chung Cheng University, Chiayi, Taiwan

REARVR: A RERAM-BASED DNN ACCELERATOR FOR MOBILE AR/VR DEVICES

Lei Zhao, Meta, Yuecheng Li, Dawei Wang, Meta, Pittsburgh, PA; Jae-sun Seo, Arizona State University, Tempe, AZ; H. Ekin Sumbul, Edith Beigne, Meta, Sunnyvale, CA

REXBDDS: REDUCTION-ON-EDGE COMPLEMENT-AND-SWAP BINARY DECISION DIAGRAMS

Gianfranco Ciardo, Andrew Miner, Lichuan Deng, Iowa State University, Ames, IA; Junaid Babar, Collins Aerospace, Cedar Rapids, IA

ROC-DRAM: LOW LATENCY AND LOW POWER DRAM USING ROWS WITH OPPOSITE CHARGING

Jaeyoon Lee, Jungrae Kim, Sungkyunkwan University, Suwon, South Korea; Daero Kim, Samsung Electronics, Suwon, South Korea

S3CURE: SCRAMBLE, SHUFFLE AND SHAMBLES – SECURE DEPLOYMENT OF MATRIX OF WEIGHTS IN MEMRISTOR CROSSBAR ARRAYS

Melvin Galicia, Ibrahim Osman, Christian Owusu-Afriyie, Rainer Leupers, RWTH Aachen University, Aachen, Germany

SHIFT-SRAM: A NOVEL ARCHITECTURE FOR ACCELERATING MAC OPERATION BY LEVERAGING BIT-WISE SPARSITY

Gaoyang Zhao, Quan Deng, Tian Zhang, Zuocheng Xing, Yaohua Wang, Yongwen Wang, National University of Defense Technology, Changsha, China

SOFTWARE-BASED FAULT-DETECTION TECHNIQUE FOR OBJECT TRACKING IN AUTONOMOUS VEHICLES

Alessio Medaglini, Sandro Bartolini, University of Siena, Italy; Gianluca Mando', Thales Italy, Sesto Fiorentino, Italy; Eduardo Quinones, Sara Royuela, Barcelona Supercomputing Center, Barcelona, Spain

SPIKE-PREDICTABLE NEURON CIRCUITS WITH ADAPTIVE THRESHOLD FOR LOW-POWER SNN SYSTEMS

Gyu Won Kam, Bohyeok Jeong, Da-Hyeon Youn, Soo Youn Kim, Dongguk University, Seoul, South Korea

STIMPACK: CONVERTIBLE NEURAL PROCESSOR SUPPORTING ADAPTIVE QUANTIZATION FOR REAL-TIME NEURAL NETWORK

Hongju Kal, Hyoseong Choi, Joon-Sung Yang, Won Woo Ro, Yonsei University, Seoul, South Korea

TECHNOLOGY MAPPING FOR BEYOND-CMOS CIRCUITRY WITH UNCONVENTIONAL COST FUNCTIONS

Dewmini Marakkalage, Siang-Yun Lee, Giovanni De Micheli, École Polytechnique Fédérale de Lausanne, Switzerland; Marcel Walter, Robert Wille, Technische Universität München, Germany

TMD-RAM: TIME-MODULATED AND DATA-AWARE IN-SRAM MAC CMOS ACCELERATOR FOR CNNs

Saeed Seyedfaraji, Salar Shakibhamedan, Baset Mesgari, Semeen Rehman, Technische Universität Wien, Vienna, Austria; Nima TaheriNejad, Heidelberg University, Heidelberg, Germany

UNREALNAS: DO NEURAL ARCHITECTURE SEARCH WITH NO LABELS

Zhen Dong, Kaicheng Zhou, Kurt Keutzer, University of California, Berkeley, CA; Guohao Li, Bernard Ghanem, KAUST, Thuwal, Saudi Arabia; Mingfei Guo, Shanghang Zhang, Peking University, Beijing, China; Qiang Zhou, Tsinghua University, Beijing, China

UNSAFE: CUNNING SENSOR ATTACK VIA FIRMWARE REVERSE-ENGINEERING

Sutej Kulkarni, Ryan Tsang, Asmita Asmita, Doreen Joseph, Sidharth Nagendran, Kevin Immanuel Gubbi, Tyler Sheaves, Houman Hodayoun, University of California, Davis, CA; Soheil Salehi, University of Arizona, Tucson, AZ

VSAGE: AN END-TO-END AUTOMATED VCO-BASED $\Delta\Sigma$ ADC GENERATOR

Ken LiTian Xie, Tzuhan Wang, Shaolan Li, Georgia Institute of Technology, Atlanta, GA

ZERO TRUST VERIFICATION OF THIRD PARTY IPS WITH SECURE MULTIPARTY COMPUTING

Zhaoxiang Liu, Xiaolong Guo, Kansas State University, Manhattan, KS; Samuel Judson, Yale University, New Haven, CT; Raj Gautam Dutta, Silicon Assurance, Gainesville, FL; Mark Santolucito, Columbia University, New York, NY

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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THURSDAY KEYNOTE: MARK HOROWITZ AND VISIONARY TALK: CECILIA METRA

Time: 8:40 AM – 10:00 AM

Event Type: Keynote

Room: 3006, 3rd Floor

INTRODUCTION AND AWARDS

AI HARDWARE RELIABILITY AND SAFETY CHALLENGES TO ENABLE THE FUTURE METAVERSE

Cecilia Metra, University of Bologna, Bologna, Italy

LIFE POST MOORE'S LAW: THE NEW CAD FRONTIER

Mark Horowitz, Stanford University, Stanford, CA

A FAREWELL TO THE NUMERICAL COMPUTING PARADIGM

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): Emerging Models of Computation

Room: 3004, 3rd Floor

Session Chair(s): Mohsen Imani, University of California, Irvine; Zheng Zhao, Synopsys

This session presents on-chip intelligence using emerging computing models that are no longer limited by numerical computing. The first two papers apply hyperdimensional computing to efficient on-chip learning, the third paper investigates architecture optimization of stochastic computing, and the last paper aims at fault tolerant design of microfluidic biochips.

LIGHTNING TALK – THE NEW ERA OF COGNITIVE COMPUTATIONAL INTELLIGENCE

Nikil Dutt, University of California, Irvine, CA

ON-DEVICE UNSUPERVISED IMAGE SEGMENTATION

Junhuan Yang, Yi Sheng, Weiwen Jiang, Lei Yang, George Mason University, Fairfax, VA; Yuzhou Zhang, Northeastern University, Seattle, WA

COMPREHENSIVE INTEGRATION OF HYPERDIMENSIONAL COMPUTING WITH DEEP LEARNING TOWARDS NEURO-SYMBOLIC AI

Hyunsei Lee, Jiseung Kim, Yeseong Kim, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea; Hanning Chen, Mohsen Imani, University of California, Irvine, CA; Ariela Zeira, Narayan Srinivasa, Intel, Santa Clara, CA

PSEUDOSC: A BINARY APPROXIMATION TO STOCHASTIC COMPUTING WITHIN LATENT OPERATION-SPACE FOR ULTRA-LIGHTWEIGHT ON-EDGE DNNs

Jihe Wang, Zhaoqing Wang, Danghui Wang, Northwestern Polytechnical University, Xi'an, China

FAULT-TOLERANCE-ORIENTED PHYSICAL DESIGN FOR FULLY PROGRAMMABLE VALVE ARRAY BIOCHIPS

Genggeng Liu, Yuhan Zhu, Wenzhong Guo, Fuzhou University, Fuzhou, China; Xing Huang, Northwestern Polytechnical University, Xi'an, China

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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BREAKING THE FAULT AND YIELD BARRIERS

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): Design for Test and Silicon Lifecycle Management

Room: 3010, 3rd Floor

Session Chair(s): Amit Majumdar, AMD

Fault detection and tolerance are crucial for today's leading-edge chips, including those using emerging devices for in-memory computing. The first paper presents an efficient approach to generate high-coverage tests at Simulink level. The next two papers advance in-memory computing by presenting an efficient fault injection technique to accelerate fault effect simulation and an efficient fault-tolerance approach to maximize chip lifetime. The last paper proposes a high-dimensional SRAM yield estimation model.

LIGHTNING TALK – ARCHITECTURE SOLUTIONS FOR EMERGING MEMORY BASED STORAGE AND COMPUTING TO ACHIEVE HIGH YIELD AND LOW ERROR RATE

Tim Cheng, Hong Kong University of Science & Technology, Hong Kong

STCG: STATE AWARE TEST CASE GENERATION FOR SIMULINK MODELS

Zhuo Su, Zehong Yu, Yu Jiang, Tsinghua University, Beijing, China; Dongyan Wang, Renmin University of China, Beijing, China; Yixiao Yang, Rui Wang, Capital Normal University, Beijing, China; Wanli Chang, University of York, United Kingdom; Aiguo Cui, Huawei, Shanghai, China

UPTIME: TOWARDS FLOW-BASED IN-MEMORY COMPUTING WITH HIGH FAULT-TOLERANCE

Sven Thijssen, Muhammad Rashedul Haq Rashed, Rickard Ewetz, University of Central Florida, Orlando, FL; Sumit Jha, The University of Texas at San Antonio, San Antonio, TX

FAULT INJECTION IN NATIVE LOGIC-IN-MEMORY COMPUTATION ON NEUROMORPHIC HARDWARE

Felix Staudigl, Thorben Fetz, Rebecca Pelke, Dominik Sisejkovic, **Jan Moritz Joseph**, Leticia Maria Bolzani Poehls, Rainer Leupers, RWTH Aachen University, Aachen, Germany

SEEKING THE YIELD BARRIER: HIGH-DIMENSIONAL SRAM EVALUATION THROUGH OPTIMAL MANIFOLD

Yanfang Liu, Wei Xing, Beihang University, Beijing, China; **Guohao Dai**, Shenzhen University, Shenzhen, China

DESIGN FOR MANUFACTURING: MAKE IT OR BREAK IT

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): Design for Manufacturing and Reliability

Room: 3002, 3rd Floor

Session Chair(s): Atsushi Takahashi, Tokyo Institute of Technology; Sandeep Kumar Samal, Intel

Design for manufacturing and yield is critical to the success of advanced nodes. This session is focused on new approaches for enhancing silicon manufacturability with better efficiency. The first paper addresses the challenge of filler cell insertion necessary for device manufacturability and performance. The next paper is on the use of discrete diffusion modeling to generate diverse layout patterns. The focus is then shifted to layout decomposition for multiple patterning lithography. The third paper uses a low-rank semi-definite programming approach with additional optimization techniques while the final paper uses an SAT-based flow to formulate a bilevel optimization problem for accuracy and speedup.

LIGHTNING TALK – DESIGN FOR MANUFACTURING: MAKE IT OR BREAK IT

To Be Announced

TOWARD OPTIMAL FILLER CELL INSERTION WITH COMPLEX IMPLANT LAYER CONSTRAINTS

Peng Zou, Guohao Chen, Jun Yu, Jianli Chen, Fudan University, Shanghai, China; Zhifeng Lin, Fuzhou University, Fuzhou, China

DIFFPATTERN: LAYOUT PATTERN GENERATION VIA DISCRETE DIFFUSION

Zixiao Wang, Wenqian Zhao, **Guojin Chen**, Farzan Farnia, Bei Yu, The Chinese University of Hong Kong, Hong Kong; Yunheng Shen, Tsinghua University, Beijing, China; Yang Bai, City University of Hong Kong, Hong Kong

LRSDP: LOW-RANK SDP FOR TRIPLE PATTERNING LITHOGRAPHY LAYOUT DECOMPOSITION

Yu Zhang, Hong Xu, Bei Yu, The Chinese University of Hong Kong, Hong Kong; Yifan Chen, Zhonglin Xie, Zaiwen Wen, Yibo Lin, Peking University, Beijing, China

LAYOUT DECOMPOSITION VIA BOOLEAN SATISFIABILITY

Hongduo Liu, Peiyu Liao, Tsung-Yi Ho, Bei Yu, The Chinese University of Hong Kong, Hong Kong; Mengchuan Zou, Bowen Pang, Mingxuan Yuan, Huawei, Hong Kong, Hong Kong; Xijun Li, University of Science and Technology of China, Shenzhen, China

Research Sessions

Special Session

Panel

Tutorial

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TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

EFFICIENT AI FOR THE EDGE: FROM HEAD TO TOE!

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): AI/ML Application and Infrastructure

Room: 3003, 3rd Floor

Session Chair(s): Yanzhi Wang, Northeastern University; Keren Zhu, The University of Texas at Austin

This session presents four papers that examine the state-of-the-art efficient AI at the edge, from low-level matrix multiplication to resource-aware inference, to parallelism and on-chip learning. The first paper proposes a new compiler plug-in for existing neural network compilers to extend their compilation ability for sparse matrix multiplication. The second paper proposes a new energy regulation framework for dynamic early exit, for active power management in neural networks inference. The third paper proposes an inter-stage parallelism optimization method to increase GPU utilization at small batch sizes, in order to accelerate edge-scale recommendation system performance. The fourth paper proposes an energy-efficient on-chip learning framework for personalized home-based rehabilitation systems.

LIGHTNING TALK – BRINGING TOGETHER FOUNDATION MODELS AND EDGE DEVICES

Yung-Hsiang Lu, Purdue University, West Lafayette, IN

SPMMPLU: A COMPILER PLUG-IN WITH SPARSE IR FOR EFFICIENT SPARSE MATRIX MULTIPLICATION

Tao Yang, Yiyuan Zhou, Qidong Tang, Feng Xu, Hui Ma, Jieru Zhao, Li Jiang, Shanghai Jiao Tong University, Shanghai, Chin

EENET: ENERGY EFFICIENT NEURAL NETWORKS WITH RUN-TIME POWER MANAGEMENT

Xiangjie Li, Yingtao Shen, An Zou, Yehan Ma, Shanghai Jiao Tong University, Shanghai, China

EAGLEREC: EDGE-SCALE RECOMMENDATION SYSTEM ACCELERATION WITH INTER-STAGE PARALLELISM OPTIMIZATION ON GPUS

Yongbo Yu, Fuxun Yu, Xiang Chen, George Mason University, Fairfax, VA; Chenchen Liu, University of Maryland, Baltimore, MD; Xiang Sheng, Amazon, Seattle, WA

ENERGY-EFFICIENT ON-CHIP TRAINING FOR CUSTOMIZED HOME-BASED REHABILITATION SYSTEMS

A. Alper Goksoy, Sizhe An, Umit Ogras, University of Wisconsin, Madison, WI

STT-RAM: STACKED, TRANSACTIONAL, AND RECONFIGURABLE MEMORIES

Time: 10:30 AM – 12:00 PM

Event Type: Research Manuscript

Topic Area(s): Embedded Memory, Storage and Networking

Room: 3006, 3rd Floor

Session Chair(s): Jason Xue, City University of Hong Kong; Preeti Ranjan Panda, Indian Institute of Technology, Delhi

This session showcases advanced memory architecture proposals, pushing the boundaries of compute-in-memory, persistence, and reconfiguration. Emerging high-bandwidth and non-volatile memories promise exciting possibilities for next generation memory systems, creating the room for innovation along many different dimensions. The papers in this session explore compute-in-memory variation of HBM, scalability of persistent transactional memory, and reconfiguration efficiencies in non-volatile FPGAs and CGRAs.

LIGHTNING TALK – CAN MEMORY TECHNOLOGIES MEET DEMANDS OF DATA ABUNDANT APPLICATIONS?

Vijay Narayanan, Pennsylvania State University, University Park, PA

LIFT: EXPLOITING HYBRID STACKED MEMORY FOR ENERGY-EFFICIENT PROCESSING OF GRAPH CONVOLUTIONAL NETWORKS

Jiaxian Chen, Zhaoyu Zhong, Kaoyi Sun, Chenlin Ma, Rui Mao, Yi Wang, Shenzhen University, Shenzhen, China

DRPTM: A DECOUPLED READ-EFFICIENT HIGH-SCALABLE PERSISTENT TRANSACTIONAL MEMORY

Wenkai Liang, Hao Hu, Xiangyu Zou, Wen Xia, **Yanqi Pan**, Harbin Institute of Technology, Shenzhen, China

CORRELATION-GUIDED PLACEMENT FOR NONVOLATILE FPGAS

Mengying Zhao, Fanjin Xu, Huichuan Zheng, **Hao Zhang**, Yuqing Xiong, Zhiping Jia, Xiaojun Cai, Shandong University, Qingdao, China

RMP-MEM: A HW/SW RECONFIGURABLE MULTI-PORT MEMORY ARCHITECTURE FOR MULTI-PEA ORIENTED CGRA

Qidie Wu, Jianguyan Gu, Youxu Lin, Tsinghua University, Beijing, China; Boxiao Han, Hongjun He, China Mobile Research Institute, Beijing, China; Yang Hu, Leibo Liu, Shaojun Wei, Shouyi Yin, Tsinghua University, Beijing, China

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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SUSTAINABLE AUTONOMOUS SYSTEMS DESIGN

Time: 10:30 AM – 12:00 PM

Event Type: Research Panel

Topic Area(s): Autonomous Systems

Room: 3014, 3rd Floor

Organizer(s): Laleh Behjat, University of Calgary, Canada

Advances in computing power have enabled exponential growth in the design of autonomous systems. These advances have impacted every aspect of our lives, from the cars we drive, to sustainable computing, to the increased use of drones, to how public transportation is built. These autonomous systems use software and hardware to ensure the safety, usability, and energy efficiency of the products. However, there has been limited debate on the principal values and objectives that need to be considered when designing such complex systems. For example, the goal of building faster vehicles can be at odds with the need to develop a sustainable transportation system.

This panel brings together leading academic and industrial experts to debate on whether the autonomous systems being designed are targeted towards a sustainable future. The panel will address the challenges associated with the following research questions:

1. How do we rethink the architecture, design, development, and deployment of autonomous systems? What are the competing objectives that need to be considered when optimizing such systems?
2. How can academic research ensure that autonomous systems are sustainable? (From funding, to talent development, to accessibility of the research)
3. How can AI and big data be used to build sustainable autonomous systems? Can it be done in a sustainable manner - for example, can the training and inference be done in an energy-efficient manner to build energy-efficient autonomous systems? What are the implications to privacy?

Moderator: Laleh Behjat, University of Calgary, Canada

Panelists: Iris Bahar, Colorado School of Mines, Golden, CO; Alex Jones, University of Pittsburgh, Pittsburgh, PA; Shiv Sikand, Drako Motors, Campbell, CA; Srilatha Manne, AMD, Seattle, WA

TECHNOLOGICAL ADVANCEMENTS IN THE QUANTUM SPACE – FROM HARDWARE ARCHITECTURE TO COMPUTING PLATFORM

Time: 10:30 AM – 12:00 PM

Event Type: Special Session (Research)

Topic Area(s): Design

Room: 3001, 3rd Floor

Organizer(s): Sabya Das, Synopsys

It is evident that Quantum Technologies are ready to take off in a big way. Quantum space is going through a major revolution across the board, starting from hardware, microarchitecture, and all the way to computing and platforms. In this session, we propose to have three complementary technologies that will cover this spectrum. In the first talk, the authors will discuss the role of the quantum system software in making erroneous quantum devices more usable and meaningful. The second topic is about NVIDIA Quantum Optimized Device Architecture (QODA), which is a single-source programming model in C++ and Python for heterogeneous quantum-classical computing. In the final presentation, the speaker will present the cryo-CMOS hardware design for the next-generation quantum computing hardware.

ROBUST RUNTIME SYSTEMS FOR SUPERCONDUCTING AND NEUTRAL ATOM BASED NOISY QUANTUM HARDWARE

Prof. Devesh Tiwari, Northeastern University, Boston, MA

CUDA QUANTUM: THE PLATFORM FOR INTEGRATED QUANTUM-CLASSICAL COMPUTING

Jin-Sung Kim, Nvidia, San Francisco, CA

PREDICTIVE ANALYTICS FOR CRYOGENIC CMOS IN FUTURE QUANTUM COMPUTING SYSTEMS

Rajiv Joshi, IBM, Yorktown Heights, NY

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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FAST BUT NOT PRECARIOUS: MEETING EFFICIENCY CHALLENGES IN AUTONOMOUS SYSTEMS

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): Autonomous Systems (Automotive, Robotics, Drones)

Room: 3003, 3rd Floor

Session Chair(s): Qi Zhu, Northwestern University, Zheng Dong, Wayne State University

Deploying autonomous systems in the wild requires meeting various challenges such as processing speed, energy consumption and low-level system errors. This session features four talks that present the latest advances in accelerator designs, model compression technique and robust training for a spectrum of components in autonomous systems, including a spatial-locality-aware tile processing unit for 3D point cloud neural networks, a semi-structured pruning method for object detection neural networks, a factor graph accelerator for motion planning, and a novel training scheme that improves bit-error robustness in reinforcement learning-enabled autonomous systems.

LIGHTNING TALK – THE NEED FOR FRUGAL AND DEPENDABLE MACHINE LEARNING

Alessandro Pinto, NASA, Berkeley, CA

TIPU: A SPATIAL-LOCALITY-AWARE NEAR-MEMORY TILE PROCESSING UNIT FOR 3D POINT CLOUD NEURAL NETWORK

Jiawei Zheng, Hao Jiang, Xinkai Nie, Zhangcheng Huang, Chixiao Chen, Qi Liu, Fudan University, Shanghai, China

R-TOSS: A FRAMEWORK FOR REAL-TIME OBJECT DETECTION USING SEMI-STRUCTURED PRUNING

Abhishek Balasubramaniam, Febin Sunny, **Sudeep Pasricha**, Colorado State University, Fort Collins, CO

BLITZCRANK: FACTOR GRAPH ACCELERATOR FOR MOTION PLANNING

Yuhui Hao, Qiang Liu, Tianjin University, Tianjin, China; Yiming Gan, Yuhao Zhu, University of Rochester, NY; Bo Yu, Shao-Shan Liu, BeyonCa, Beijing, China

BERRY: BIT ERROR ROBUSTNESS FOR ENERGY- EFFICIENT REINFORCEMENT LEARNING-BASED AUTONOMOUS SYSTEMS

Zishen Wan, Arijit Raychowdhury, Georgia Institute of Technology, Atlanta, GA; Nandhini Chandramoorthy, Karthik Swaminathan, Pin-Yu Chen, IBM Research, Yorktown Heights, NY; Vijay Reddi, Harvard University, Cambridge, MA

LET'S GET WITH THE PROCESSING-IN- MEMORY PROGRAM

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): In-memory and Near-memory Computing Architectures, Applications and Systems

Room: 3004, 3rd Floor

Session Chair(s): Rajesh Jayashankara Shridevi, Intel; Florian Zaruba, Axelera AI

Processing in Memory (PIM) has been around for decades, but adoption has been slow in large part due to programming challenges. The performance and energy benefits of performing computations in DRAM or storage are evident, yet these techniques have not been widely commercialized. PIM does not have direct access to important features within CPUs, such as address translation and atomic instructions. These programming challenges must be solved for PIM to reach its potential. This session looks to advance research in this area using features such as fine-grained acceleration and CXL.

LIGHTNING TALK – MEMORY-CENTRIC COMPUTING

Onur Mutlu, ETH Zürich, Switzerland

VPIM: EFFICIENT VIRTUAL ADDRESS TRANSLATION FOR SCALABLE PROCESSING IN-MEMORY ARCHITECTURES

Amel Fatima, Korakit Seemakhupt, Samira Khan, University of Virginia, Charlottesville, VA; Sihang Liu, University of Waterloo, Canada; Rachata Ausavarungnirun, King Mongkut's University of Technology North Bangkok, Thailand

PUMICE: PROCESSING-USING-MEMORY INTEGRATION WITH A SCALAR PIPELINE FOR SYMBIOTIC EXECUTION

Socrates Wong, Cecilio Tamarit, José Martínez, Cornell University, Ithaca, NY

HARDWARE SUPPORT FOR DURABLE ATOMIC INSTRUCTIONS FOR PERSISTENT PARALLEL PROGRAMMING

Khan Shaikhul Hadi, Naveed Mustafa, Mark Heinrich, Yan Solihin, University of Central Florida, Orlando, FL

SIDEKICK: NEAR DATA PROCESSING FOR CLUSTERING ENHANCED BY AUTOMATIC MEMORY DISAGGREGATION

Sanghoon Lee, **Jongho Park**, Yeseong Kim, Daegu Gyeongbuk Institute of Science and Technology, Dalseong, South Korea; Minh Ha, Byung Koh, Kyoung Park, SK hynix, Incheon, South Korea

Research
Sessions

Special
Session

Panel

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Hands-on Labs

Transformative
Technologies
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TechTalk
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Keynotes and
Visionary Talks

Engineering
Track

NASA IN DAC?

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): Design Methodologies for System-on-Chip and 3D/2.5D System-in Package

Room: 3006, 3rd Floor

Session Chair(s): Ujjwal Guin, Auburn University; Peipei Zhou, University of Pittsburgh

At the first DAC in 1964, papers were typed on typewriters and tools were described as working on designs of arbitrary size, as long as there were no more than 20 transistors. Today, in DAC 60, while we handle many more characteristics for much larger designs, how do we address new design challenges and explore the vast design space in a “universe” of design parameters? “NASA in DAC” will launch “crewed spacecrafts” with “interstellar” missions to explore four “stars”: (1) CPU, (2) Systolic Array Designs in FPGA, (3) Heterogeneous SoC with FPGA+ASICs+CPU and (4) ASICs for TinyML. “Fasten your seat belts for a space visit: we are going to travel to outer space!”

LIGHTNING TALK – NASA IN DAC?

Avinash Karanthi, Ohio University, Athens, OH

A HIGH-ACCURATE MULTI-OBJECTIVE EXPLORATION FRAMEWORK FOR DESIGN SPACE OF CPU

Duo Wang, Mingyu Yan, Xin Liu, Mo Zou, Tianyu Liu, Wenming Li, Xiaochun Ye, Dongrui Fan, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

A COMPREHENSIVE AUTOMATED EXPLORATION FRAMEWORK FOR SYSTOLIC ARRAY DESIGNS

Suhail Basalama, Jie Wang, Jason Cong, University of California, Los Angeles, CA

HIGH PERFORMANCE, LOW POWER MATRIX MULTIPLY DESIGN ON ACAP: FROM ARCHITECTURE, DESIGN CHALLENGES AND DSE PERSPECTIVES

Jinming Zhuang, Zhuoping Yang, Peipei Zhou, University of Pittsburgh, PA

A MODEL-SPECIFIC END-TO-END DESIGN METHODOLOGY FOR RESOURCE-CONSTRAINED TINYML HARDWARE

Yanchi Dong, Tianyu Jia, Kaixuan Du, Yiqi Jing, Yufei Ma, Yun Liang, Le Ye, Ru Huang, Peking University, Beijing, China; Qijun Wang, Pixian Zhan, Yadong Zhang, Fengyun Yan, Nano Core Chip Electronic Technology, Hangzhou, China

PROGRESS FROM THE LEADING EDGE OF RTL SYNTHESIS

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s): RTL/Logic Level and High-level Synthesis

Room: 3002, 3rd Floor

Session Chair(s): Yukio Miyasaka, University of California, Berkeley; Eleonora Testa, Synopsys

Challenging contributions from approximate logic synthesis by means of non-conflicting multiple local approximation changes, from technology mapping based on structural choices on non-overlapping subgraphs, and from an optimization framework to design multiplier based on reinforcement learning. Last but not least, a general EDA optimization scheme based on analytic gradient-descent without reinforcement learning: its success in the case of gate sizing opens new perspectives where reinforcement learning suffers from sample inefficiency and limited generalization.

LIGHTNING TALK – LATEST TRENDS IN INDUSTRIAL LOGIC SYNTHESIS

Luca Amaru, Synopsys, San Francisco, CA

ACCALS: ACCELERATING APPROXIMATE LOGIC SYNTHESIS BY SELECTION OF MULTIPLE LOCAL APPROXIMATE CHANGES

Xuan Wang, Sijun Tao, Jingjing Zhu, Weikang Qian, Shanghai Jiao Tong University, Shanghai, China; Yiyu Shi, University of Notre Dame, Notre Dame, IN

LIGHTWEIGHT STRUCTURAL CHOICES OPERATOR FOR TECHNOLOGY MAPPING

Antoine Grosnit, Matthieu Zimmer, Rasul Tutunov, Haitham Bou Ammar, Huawei, London, United Kingdom; Xing Li, Lei Chen, Mingxuan Yuan, Huawei, Hong Kong, Hong Kong; Fan Yang, Huawei Hisilicon, Shenzhen, China

AGD: A LEARNING-BASED OPTIMIZATION FRAMEWORK FOR EDA AND ITS APPLICATION TO GATE SIZING

Phuoc Pham, Jaeyong Chung, Incheon National University, Incheon, South Korea

RL-MUL: MULTIPLIER DESIGN OPTIMIZATION WITH DEEP REINFORCEMENT LEARNING

Dongsheng Zuo, Yikang Ouyang, Yuzhe Ma, The Hong Kong University of Science and Technology Guangzhou, China

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

THIS IS FORMAL...BUT YOU CAN COME CASUAL!

Time: 1:30 PM – 3:00 PM

Event Type: Research Manuscript

Topic Area(s):

Room: 3010, 3rd Floor

Session Chair(s): Prabhat Mishra, University of Florida; Maheshwar Chandrasekar, Synopsys

This session covers checking and formal verification techniques. A brand new technique for sequential equivalence checking without the restriction of cycle accuracy that is elegant and performant. A new way to think of verification of dividers- functional abstractions without the memory overhead of arithmetic rewriting. An extension of basic accelerator verification to incorporate interfering actions. An end to end checking procedure for complex fully homomorphic encryption engines inspired by compiler design techniques.

LIGHTNING TALK – A PERSPECTIVE ON FORMAL VERIFICATION

Karim Khordoc, NVIDIA, Ottawa, Canada

SE3: SEQUENTIAL EQUIVALENCE CHECKING FOR NON-CYCLE-ACCURATE DESIGN TRANSFORMATIONS

You Li, Guannan Zhao, Yunqi He, Hai Zhou, Northwestern University, Evanston, IL

FORMAL VERIFICATION OF RESTORING DIVIDERS MADE FAST AND SIMPLE

Jiteshri Dasari, Maciej Ciesielski, University of Massachusetts, Amherst, MA

G-QED: GENERALIZED QED PRE-SILICON VERIFICATION BEYOND NON-INTERFERING HARDWARE ACCELERATORS

Saranyu Chattopadhyay, Florian Lonsing, Brandon D’Agostino, Ioanna Vavelidou, Caroline Trippel, Clark Barrett, Subhasish Mitra, Stanford University, CA; Keerthikumara Devarajegowda, Siemens EDA, Neubiberg, Germany; Bihan Zhao, Vijay Bhatt, Sebastian Prebeck, Wolfgang Ecker, Infineon Technologies, Neubiberg, Germany

TOWARDS A FORMALLY VERIFIED FULLY HOMOMORPHIC ENCRYPTION COMPUTE ENGINE

Jeremy Casas, Zhenkun Yang, Wen Wang, Jin Yang, Intel, Hillsboro, OR; Adwait Godbole, University of California, Berkeley, CA

HIGH-LEVEL SYNTHESIS: NOW IS THE TIME OR WILL IT CONTINUE TO REMAIN JUST A PROMISING TECHNOLOGY?

Time: 1:30 PM – 3:00 PM

Event Type: Research Panel

Topic Area(s): EDA

Room: 3014, 3rd Floor

Organizer(s): Sabya Das, Synopsys, San Francisco, CA;

Today’s state of the art designers are taking a close look at the High-Level synthesis (HLS) technology. With the advent of new process nodes, complexity of the design, and faster time-to-market for large SOCs, HLS is getting another chance to become part of the primary design methodology.

In the past 30 years, there was a technological push to make HLS mainstream. However, those attempts were not very successful, and hardware companies continued to rely on the RTL-based design-entry methodology. As a result, HLS always remained as the promising technology that will be deployed everywhere, only in future.

In this panel, the experts will debate whether now is the time of HLS or not. While nobody discards the technological advancement of High-Level synthesis, the debate will be primarily centered around whether HLS will continue to remain as the promising kid, that did not deliver to the expectation or hype.

Moderator: Jason Anderson, University of Toronto, Canada

Panelists: Rajesh Gupta, University of California, San Diego, La Jolla, CA; Janet Olson, Cadence Design Systems, Inc., Saratoga, CA; Abhijeet Chakraborty, Synopsys, San Francisco, CA; Zhiru Zhang, Cornell University, Ithaca, NY; Priyanka Raina, Stanford University, Stanford, CA

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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PRE-SILICON PHYSICAL SECURITY VERIFICATION: FINDING HAYSTACK NEEDLES BEFORE THEY STING

Time: 1:30 PM – 3:00 PM

Event Type: Special Session (Research)

Topic Area(s): Security

Room: 3001, 3rd Floor

Organizer(s): Patrick Schaumont, Worcester Polytechnic Institute, Worcester, MA

Modern SoC design has enabled integration of functionality at a cost of increased complexity, cost, and risk. Traditional security evaluation of these chips uses prototype certification where an evaluator tries to identify vulnerabilities through testing. However, this method only provides an overall assessment and doesn't identify root causes. Pre-silicon security verification offers an opportunity to detect vulnerabilities early through modeling, simulation, and formal verification. This approach provides root cause analysis and eliminates vulnerabilities from implementation.

This session presents solutions for hunting known hardware security vulnerabilities such as unwanted information leakage, faults, priority escalation, and potential tamper or Trojans. Industry experts will discuss opportunities and challenges in pre-silicon security verification, with a focus on the gap between academic theory and practical deployment. The 90-minute session includes three talks.

1. Jasper van Woudenberg from Riscure presents "Gone in 60M seconds: Challenges for Presilicon SCA and FI simulations" discussing the transition from traditional security evaluation to pre-silicon evaluation and the challenges in building usable tools.
2. Peter Grossmann from Zero ASIC Corporation presents "Unleashing Side-channel Power Estimation Super Powers" describing improvements to power estimation techniques for pre-silicon side-channel leakage evaluation.
3. Avinash L Varna from Intel presents "Pre-Silicon Security Assurance for SCA and FI: Turning Research into Industrial Practice" reviewing the challenges of integrating pre-silicon security testing into industrial design and verification flows.

GONE IN 60M SECONDS: CHALLENGES FOR PRESILICON SCA AND FI SIMULATIONS

Jasper van Woudenberg, Riscure, San Francisco, CA

UNLEASHING SIDE-CHANNEL POWER ESTIMATION SUPER POWERS

Peter Grossman, Zero ASIC, Boston, MA

PRE-SILICON SECURITY ASSURANCE FOR SCA AND FI: AN INDUSTRY PERSPECTIVE

Avinash Varna, Intel, Chandler, AZ

* Denotes a Best Paper Candidate

"KNOW THY SELF, KNOW THY ENEMY: HW SECURITY ATTACKS AND DEFENSES"

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Hardware Security: Attack and Defense

Room: 3003, 3rd Floor

Session Chair(s): Xiaolong Guo, Kansas State University; Domenic Forte, University of Florida

In the last decade or so, research in hardware security has led to the discovery of hardware-oriented weaknesses that can be exploited remotely, in the supply chain, or through physical access. This session consists of papers that acknowledge and deal with at least one of these threats. In the areas of microarchitectural security and non-invasive attacks, the first 3 presentations discuss launching and detecting side-channel and interrupt-based attacks. To address supply chain risks, the last 3 papers propose CAD/EDA-based mitigations against hardware Trojan insertion and ML-based logic locking attacks.

LIGHTNING TALK – UNLOCKING THE POTENTIAL OF THE ANALOG DOMAIN: EXPLORING THE NEXT FRONTIER IN HARDWARE SECURITY

Waleed Khalil, The Ohio State University, Columbus, OH

CHAOSINTC: A SECURE INTERRUPT MANAGEMENT MECHANISM AGAINST INTERRUPT-BASED ATTACKS ON TEE

Yifan Zhu, Peinan Li, Lutan Zhao, Dan Meng, Rui Hou, Institute of Information Engineering, Chinese Academy of Sciences, Beijing, China

SCAGUARD: DETECTION AND CLASSIFICATION OF CACHE SIDE-CHANNEL ATTACKS VIA ATTACK BEHAVIOR MODELING AND SIMILARITY COMPARISON

Limin Wang, Lei Bu, Nanjing University, Nanjing, China; Fu Song, Shanghai Tech University, Shanghai, China

*AVX TIMING SIDE-CHANNEL ATTACKS AGAINST ADDRESS SPACE LAYOUT RANDOMIZATION

Hyunwoo Choi, The Affiliated Institute of ETRI, Daejeon, South Korea; Suryeon Kim, Korea Seungwon Shin, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea

GDSII-GUARD: ECO ANTI-TROJAN OPTIMIZATION WITH EXPLORATORY TIMING-SECURITY TRADE-OFFS

Xinming Wei, Jiaxi Zhang, Guojie Luo, Peking University, Beijing, China

ALMOST: ADVERSARIAL LEARNING TO MITIGATE ORACLE-LESS ML ATTACKS VIA SYNTHESIS TUNING

Animesh Basak Chowdhury, Luca Collini, Ramesh Karri, Siddharth Garg, New York University, New York, NY; Lilas Alrahis, Johann Knechtel, Ozgur Sinanoglu, New York University, Abu Dhabi, United Arab Emirates; Benjamin Tan, University of Calgary, Canada

SIMLL: SIMILARITY-BASED LOGIC LOCKING AGAINST MACHINE LEARNING ATTACKS

Subhajit Dutta Chowdhury, Kaixin Yang, Pierluigi Nuzzo, University of Southern California, Los Angeles, CA

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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“ML UNDER ATTACK, AND ML FOR ATTACKS AND DEFENSES”

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Hardware Security: Attack and Defense

Room: 3002, 3rd Floor

Session Chair(s): Fan Yao, University of Central Florida

Centrality of ML models to modern systems makes attacks on the correctness of their execution highly impactful. This session explores the interplay between ML algorithms and system security. The first two papers in the session focus on defenses against such attacks on ML models. The next three papers explore how ML algorithms both endanger existing security and help with inventing new defenses. The final paper identifies an attack on a popular embedded architecture.

LIGHTNING TALK – “ML UNDER ATTACK, AND ML FOR ATTACKS AND DEFENSES”

Farinaz Koushanfar, University of California, San Diego, San CA

HAMMERDODGER: A LIGHTWEIGHT DEFENSE FRAMEWORK AGAINST ROWHAMMER ATTACK ON DEEP NEURAL NETWORKS

Cheng Gongye, Yukui Luo, Xiaolin Xu, Yunsi Fei, Northeastern University, Boston, MA

NTESTING: NEURAL NETWORK FAULT ATTACKS DETECTION USING GRADIENT-BASED TEST VECTOR GENERATION

Antian Wang, Bingyin Zhao, Yingjie Lao, Clemson University, Clemson, SC; Weihang Tan, University of Minnesota, Twin Cities, Minneapolis, MN

EXPLOREFAULT: IDENTIFYING EXPLOITABLE FAULT MODELS IN BLOCK CIPHERS WITH REINFORCEMENT LEARNING

Hao Guo, Vasudev Gohil, Satwik Patnaik, Jeyavijayan Rajendran, Texas A&M University, College Station, TX; Sayandeep Saha, Debdeep Mukhopadhyaya, Indian Institute of Technology, Kharagpur, India

POWER SIDE-CHANNEL VULNERABILITY ASSESSMENT OF LIGHTWEIGHT CRYPTOGRAPHIC SCHEME, XOODYAK

Anupam Golder, Georgia Institute of Technology, Atlanta, GA; Debayan Das, Santosh Ghosh, Sayak Ray, Jason Fung, Intel, Hillsboro, OR; Avinash Varna, Daniel Dinu, Intel, Chandler, AZ; Majid Sabbagh, Northeastern University, Boston, MA; Rana Elnaggar, Duke University, Durham, NC; Joseph Friel, Intel, Austin, TX

DISCERNING THE LIMITATIONS OF GNN-BASED ATTACKS ON LOGIC LOCKING

Armin Darjani, Nima Kavand, **Shubham Rai**, Akash Kumar, Technische Universität Dresden, Germany

RETURN-TO-NON-SECURE VULNERABILITIES ON ARM CORTEX-M TRUSTZONE: ATTACK AND DEFENSE

Zheyuan Ma, Xi Tan, Lukasz Ziarek, Hongxin Hu, Ziming Zhao, University at Buffalo, Buffalo, NY; Ning Zhang, Washington University, St. Louis, MO

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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INFUSING INTELLIGENCE INTO EMBEDDED SOFTWARE

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Embedded Software

Room: 3006, 3rd Floor

Session Chair(s): Chen Pan, Texas A&M University, Corpus Christi

This session covers advancements in adoption and optimization of deep learning techniques for embedded software on resource constrained platforms. The first paper presents reinforcement learning based configuration tuning for DSP compilers. The next two papers employ deep learning for indoor localization using smartphones and SSD resource allocation. The final three papers focus on improving the efficiency and privacy of neural network accelerators on embedded hardware.

LIGHTNING TALK – CO-DESIGN AND CHARACTERIZATION OF AI/ML EMBEDDED SOFTWARE FOR ULTRA-LOW POWER PLATFORMS

David Atienza, *École Polytechnique Fédérale de Lausanne, Switzerland*

AUTOMATIC END-TO-END JOINT OPTIMIZATION FOR KERNEL COMPILATION ON DSPS

Xiaolei Zhao, *Zhaoyun Chen, Yang Shi, Mei Wen, Chunyuan Zhang, National University of Defense Technology, Changsha, China*

VITAL: VISION TRANSFORMER NEURAL NETWORKS FOR SMARTPHONE HETEROGENEITY RESILIENT AND ACCURATE INDOOR LOCALIZATION

Danish Gufran, *Saideep Tiku, Sudeep Pasricha, Colorado State University, Fort Collins, CO*

RLALLOC: A DEEP REINFORCEMENT LEARNING-ASSISTED RESOURCE ALLOCATION FRAMEWORK FOR ENHANCED BOTH I/O THROUGHPUT AND QOS PERFORMANCE OF MULTI-STREAMED SSDS

Mengquan Li, Kenli Li, Hunan University, Changsha, China; Chao Wu, Northeastern University, Boston, MA; Congming Gao, Xiamen University, Xiamen, China; Cheng Ji, Nanjing University of Science and Technology, Nanjing, China

TOWARDS EFFICIENT CONVOLUTIONAL NEURAL NETWORK FOR EMBEDDED HARDWARE VIA MULTI-DIMENSIONAL PRUNING

Hao Kong, *Xiangzhong Luo, Shuo Huai, Weichen Liu, Nanyang Technological University, Singapore; Di Liu, Norwegian University of Science and Technology, Trondheim, Norway; Ravi Subramaniam, Christian Makaya, Qian Lin, Hewlett Packard Enterprise, Palo Alto, CA*

HTVM: EFFICIENT NEURAL NETWORK DEPLOYMENT ON HETEROGENEOUS TINYML PLATFORMS

Josse Van Delm, *Maarten Vandersteegen, Giuseppe Sarda, Marian Verhelst, KU Leuven, Belgium; Alessio Burrello, Francesco Conti, Luca Benini, University of Bologna, Italy; Daniele Jahier Pagliari, Politecnico di Torino, Italy*

PRIVACY-PRESERVING DNN TRAINING WITH PREFETCHED META-KEYS ON HETEROGENEOUS NEURAL NETWORK ACCELERATORS

Qiushi Li, Ju Ren, Yaoxue Zhang, Tsinghua University, Beijing, China; Yan Zhang, China Agricultural University, Beijing, China; Chengru Song, Yiqiao Liao, Kuaishou Inc., Beijing, China

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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TESTING, THEN JUMPING INTO THE DEEP (LEARNING) END

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Design Verification and Validation

Room: 3010, 3rd Floor

Session Chair(s): Yangdi Lyu, The Hong Kong University of Science and Technology, Guangzhou

This session covers deep learning synthesis and novel testing approaches. A meta reinforcement learning approach to synthesize deep neural network controllers. Learning higher order abstractions from bit blasted Boolean networks with graph neural networks. GPUs to fuzz multiple hardware inputs faster than ever before. An open sourced, mutation testing tool for hardware designs. A testing approach that can find real bugs in Simulink code generation.

LIGHTNING TALK – FUNCTIONAL VERIFICATION – PAST, PRESENT, AND FUTURE CHALLENGES AND OPPORTUNITIES

Avi Ziv, IBM, THaifa, Israel

SAFE DNN-TYPE CONTROLLER SYNTHESIS FOR NONLINEAR SYSTEMS VIA META REINFORCEMENT LEARNING

Hanrui Zhao, Niuniu Qi, Zhengfeng Yang, East China Normal University, Shanghai, China; Xia Zeng, Southwest University, Chongqing, China; Zhenbing Zeng, Shanghai University, Shanghai, China

*GAMORA: GRAPH LEARNING BASED SYMBOLIC REASONING FOR LARGE-SCALE BOOLEAN NETWORKS

Nan Wu, Yuan Xie, University of California, Santa Barbara, CA; Yingjie Li, Cunxi Yu, University of Utah, Salt Lake City, UT; Cong “Callie” Hao, Georgia Institute of Technology, Atlanta, AL; Steve Dai, NVIDIA, Santa Clara, CA

GENFUZZ: GPU-ACCELERATED HARDWARE FUZZING USING GENETIC ALGORITHM WITH MULTIPLE INPUTS

Dian-Lun Lin, Shih-Hsin Wang, Tsung-Wei Huang, University of Utah, Salt Lake City, UT; Yanqing Zhang, NVIDIA, Santa Clara, CA; Haoxing Ren, NVIDIA, Austin, TX; Brucek Khailany, NVIDIA, Austin, TX

PARTITION BASED DIFFERENTIAL TESTING FOR FINDING EMBEDDED CODE GENERATION BUGS IN SIMULINK

He Jiang, Dalian University of Technology, Dalian, China; Hongyi Cheng, Shikai Guo, **Xiaochen Li**, Dalian University of Technology, Dalian, China

MANTRA: MUTATION TESTING OF HARDWARE DESIGN CODE BASED ON REAL BUGS

Jiang Wu, Deheng Yang, Pan Li, Jiayu He, Xiaoguang Mao, National University of Defense Technology, Changsha, China; Yan Lei, Chongqing University, Chongqing, China; Zhuo Zhang, Ningbo Industrial Internet Research Institute, Ningbo, China; Xiankai Meng, Shanghai Polytechnic University, Shanghai, China

* Denotes a Best Paper Candidate

GENERAL-PURPOSE GATE-LEVEL SIMULATION WITH PARTITION-AGNOSTIC PARALLELISM

Zizheng Guo, Zuodong Zhang, Xun Jiang, Yibo Lin, Runsheng Wang, Ru Huang, Peking University, Beijing, China; Wuxi Li, AMD, San Jose, CA

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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PROGRAM

Thursday, July 13, 2023

THE PATH TO RELIABLE, SECURE, AND ENERGY-EFFICIENT CLOUD-EDGE CONTINUUM

Time: 3:30 PM – 5:30 PM

Event Type: Research Manuscript

Topic Area(s): Design of Cyber-physical Systems and IoT

Room: 3004, 3rd Floor

Session Chair(s): Hiroki Matsutani, Keio University; Karthi Duraisamy, Synopsys

This session focuses on the design of Cyber-Physical Systems (CPS) and the Internet of Things (IoT). The papers in this session address important issues related to CPS sensing, scheduling, reliability, criticality, energy-efficiency, and verification. By participating in this session, attendees will gain a comprehensive understanding of modern CPS and IoT solutions, including autonomous systems, 5G-industry applications, and Augmented Reality (AR)/Virtual Reality (VR) applications. This session promises to be a unique learning experience, providing attendees with the knowledge they need to comprehend the complexities of CPS and IoT design.

LIGHTNING TALK – THE PATH TO RELIABLE, SECURE, AND ENERGY-EFFICIENT CLOUD-EDGE CONTINUUM

Susmit Jha, SRI, San Francisco, CA

MEMORY-EFFICIENT AND REAL-TIME SPAD-BASED DTOF IMAGING WITH SPATIAL AND STATISTICAL CORRELATION

Shiyao Li, Zhenhua Zhu, Yu Zhu, Jiangwei Zhang, Huazhong Yang, Yu Wang, Tsinghua University, Beijing, China; Qingpeng Zhu, Wenxiu Sun, SenseTime Research and Tetras.AI, Shenzhen, China; Guohao Dai, Shanghai Jiao Tong University, Shanghai, China; Fei Qiao, Beijing National Research Center for Information Science and Technology, Beijing, China

WORK OR SLEEP: FRESHNESS-AWARE ENERGY SCHEDULING FOR WIRELESS POWERED COMMUNICATION NETWORKS WITH INTERFERENCE CONSIDERATION

Ling Lin, Lei Ju, Wei Zhang, **Zimeng Zhou**, Shandong University, Qingdao, China; Jason Xue, City University of Hong Kong; Mingliang Zhou, Chongqing University, Chongqing, China

APP: ENABLING SOFT REAL-TIME EXECUTION ON DENSELY-POPULATED HYBRID MEMORY SYSTEMS

Zheng-Wei Wu, **Yun-Chih Chen**, Tei-Wei Kuo, National Taiwan University, Taipei, Taiwan; Yuan-Hao Chang, Academia Sinica, Taipei, Taiwan

SHOGGOTH: TOWARDS EFFICIENT EDGE-CLOUD COLLABORATIVE REAL-TIME VIDEO INFERENCE VIA ADAPTIVE ONLINE LEARNING

Liang Wang, Kai Lu, Jiguang Wan, Guikuan Li, Huazhong University of Science and Technology, Wuhan, China; Nan Zhang, Xiaoyang Qu, Jianzong Wang, Jing Xiao, Ping An Technology, Shenzhen, China

CONTENTION-FREE CONFIGURED GRANT SCHEDULING FOR 5G URLLC TRAFFIC

Tianyu Zhang, Song Han, University of Connecticut, Storrs, CT; X. Sharon Hu, University of Notre Dame, South Bend, IN

SEO: SAFETY-AWARE ENERGY OPTIMIZATION FRAMEWORK FOR MULTI-SENSOR NEURAL CONTROLLERS AT THE EDGE

Mohanad Odema, James Ferlez, Yasser Shoukry, Mohammad Al Faruque, University of California, Irvine, CA

Research Sessions	Special Session	Panel	Tutorial	Workshop; Hands-on Labs	Transformative Technologies Theater	DAC Pavilion Panel; Analyst Review	TechTalk SKYTalk	Keynotes and Visionary Talks	Engineering Track
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ACHIEVING VERIFIABLE AUTONOMY: IS DESIGN AUTOMATION THE GOLDEN KEY?

Time: 3:30 PM – 5:30 PM

Event Type: Research Panel

Topic Area(s): Autonomous Systems

Room: 3014, 3rd Floor

Organizer/Moderator: Samarjit Chakraborty, University of North Carolina, Chapel Hill, NC

In many domains, and in particular in the automotive domain, we have already overcome several technical challenges on the path towards implementing autonomous systems. However, practical realization and mass adoption of autonomous systems and vehicles still remains elusive. One of the fundamental remaining obstacles is to ensure that the system behaves correctly in all possible scenarios – a goal that needs to be achieved via formal or semi-formal verification.

But the complexity of most autonomous systems makes this a very hard final challenge. In particular, traditional abstractions and well-tested principles that follow the “separation of concerns” paradigm to manage complexity, no longer seem to work. For example, fully verifying machine learning (ML) based perception processing subsystems in isolation might not be feasible. But when such perception processing is viewed in conjunction with the control components they feed into, full verification of the ML components might not be necessary to provide “global” correctness guarantees. Similarly, while high-level models of control components can be formally verified today, verifying software implementations synthesized from such models, especially when they are running on complex distributed architectures is more difficult. Building simulations and virtual prototypes are both difficult and expensive and still do not offer the kind of guarantees that are necessary. Along the same lines, while the real-time systems literature provides an array of formal methods for timing analysis and scheduling, few of them scale to the complexity found in real-life autonomous systems.

In summary, addressing the verification challenge for autonomous systems requires more holistic approaches that can “connect” different subsystems together for design, optimization, and verification. Such cross-layer verification requires design automation and suitable design tools. Do such tools and methods already exist? Which gaps in the availability of design automation tools are already recognized in the industry? What kinds of scientific challenges in developing such necessary tool support is recognized by the academic research community? And most fundamentally, does design automation indeed hold the key to achieving verifiable autonomy without overprovisioning resources?

The goal of this panel would be to discuss and debate on these questions. It will shed light on perspectives of the academic research community and also that of the industry. The outcome of this panel discussion would be an actionable research agenda for embedded systems and design automation researchers.

Panelists: Nikil Dutt, University of California, Irvine, CA; Insup Lee, University of Pennsylvania, PA; Unmesh Bordoloi, Siemens EDA, San Diego, CA; Ramesh S., General Motors, Warren, MI

WILL HETEROGENEOUS INTEGRATION DRIVE THE NEXT PHASE OF MOORE’S LAW?

Time: 3:30 PM – 5:30 PM

Event Type: Special Session (Research)

Topic Area(s): EDA

Room: 3001, 3rd Floor

Organizer(s): Muhannad Bakir, Georgia Institute of Technology; Saibal Mukhopadhyay, Georgia Institute of Technology

Packaging in the new era of Moore’s Law will offer extreme levels of die integration/bonding and begin to blur the boundary between on- and off-chip connectivity (especially in 3D architectures) due to ever denser physical I/O interfaces/bonds. This new form of ‘packaging’ is often referred to as ‘Heterogeneous Integration’ or HI today. A common goal for HI is to enable the interconnection of multiple dice (or “chiplets”) of various functionalities in a manner that approaches monolithic-like performance yet utilizes advanced off-chip interconnects and packaging/ assembly to provide flexibility in IC fabrication and design, improved scalability, reduced development time, and reduced cost. In fact, a cost-benefit analysis of monolithic die disaggregation was recently performed at the 3 nm node and showed that chiplets become cost competitive when monolithic die size exceeds 150 mm² due to yield considerations of larger monolithic die [1].

The aim of this session is look at emerging technologies and extreme HI architectures that seek to eliminate the boundaries between on-chip and off-chip connectivity.

[1] K. Kim, “The smallest engine transforming humanity: the past, present, and future,” in Proc. IEEE International Electron Devices Meeting (IEDM), 2021

ADVANCED PACKAGING DESIGN CHALLENGES FOR HETEROGENEOUS INTEGRATION

CP Hung, ASE Group, Kaohsiung, Taiwan

ADVANCED PACKAGING AND INTEGRATION: IT’S NOT ENOUGH

Gabriel Loh, AMD, Bellevue, WA

BURIED POWER RAILS

Jaydeep Kulkarni, The University of Texas at Austin, TX

DESIGN AUTOMATION NEEDS FOR MONOLITHIC 3D ICs: ACCOMPLISHMENTS AND GAPS

Sung Kyu Lim, Georgia Institute of Technology, Atlanta, GA

Research Sessions

Special Session

Panel

Tutorial

Workshop; Hands-on Labs

Transformative Technologies Theater

DAC Pavilion Panel; Analyst Review

TechTalk SKYTalk

Keynotes and Visionary Talks

Engineering Track

ADDITIONAL MEETINGS

HACK at DAC

Sunday, July 9 – Monday, July 10

8:00 am – 6:00 pm

Level 2 Lobby

Early Career Workshop

Sunday, July 9

9:00 am – 5:00 pm

Room 3016

Young Fellows Program

Sunday, July 9

9:00 am – 6:00 pm

Room 3018

Monday, July 10

7:00 pm – 9:00 pm

Level 2 Lobby

Thursday, July 13

3:30 pm – 5:30 pm

Room 3008

Needham Presentation

Sunday, July 9

5:00 pm – 6:00 pm

Room 3002

TODAES Editorial Board Meeting

Monday, July 10

10:30 am – 12:00 pm

Room 3010

ACM Annual Meeting

Monday, July 10

2:00 pm – 6:00 pm

Room 3010

Cooley's DAC Troublemaker Panel

Monday, July 10

3:00 pm – 4:00 pm

Room 3016

PhD Forum and University Demo

Monday, July 10

7:00 pm – 9:00 pm

Level 2 Lobby

CEDA IEEE Distinguished Lecture Luncheon

Tuesday, July 11

12:00 pm – 1:30 pm

Room 3018

Doulos Lunch'n'Learn

Wednesday, July 12

12:00 pm – 1:30 pm

Room 3016

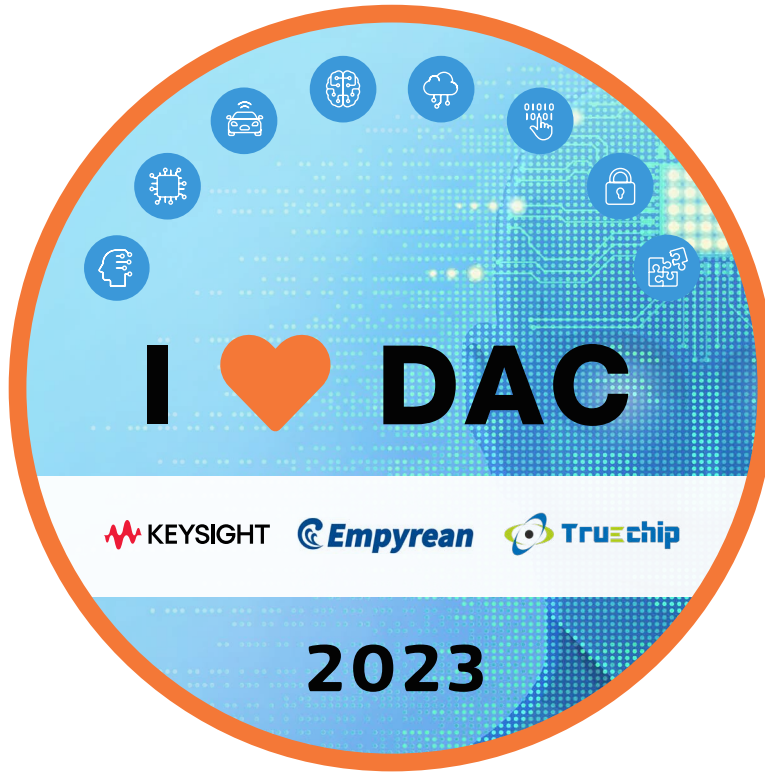
Birds of a Feather

Wednesday, July 12

6:00 pm – 9:30 pm

Room 3001

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Booth 1531



Booth 2537



Booth 2544

TRANSFORMATIVE TECHNOLOGIES THEATER

Booth #1358

MONDAY, JULY 10TH	
10:30 am – 11:15 am	Cloud but not for Compute – A New Paradigm for Open IC Design Mohamed Kassem, eFabless
11:30 am – 12:00 pm	Digital Transformation Platform for Electronics Hardware Ted Pawela, Altium, Inc.
12:15 pm – 12:45 pm	Chip Design – Cloud & Efficiency Di Wu, Shengke Zhou, Tianheng Tu, Google Cloud
1:00 pm – 1:45 pm	Panel: The Good, Bad and Cloudy Ann Mutschler, Semiconductor Engineering; Rob Aitken, Synopsys; Mahesh Turaga, Cadence; Craig Johnson, Siemens EDA; Richard Ho, Lightmatter; Phil Steinke, AMD
2:00 pm – 2:30 pm	Simplifying Success in the Cloud Craig Johnson, Siemens
2:45 pm – 3:15 pm	Tropos Platform – A Novel DevSecOps Platform for IC/FPGA Design Vamshi Reddy, Tuple Tech
3:30 pm – 4:15 pm	Ask My Anything with Sean Jensen-Grey Sean Jensen-Grey, Google
4:30 pm – 5:00 pm	Hybrid Cloud Bursting In Enterprises Alok Sinha, Spillbox; Jaideep Sen, Spillbox
5:15 pm – 5:45 pm	Maximize Designer Productivity through Microsoft's New Cloud Native, On-demand, Secure Collaborative Design Environment Prashant Varshney, Microsoft
TUESDAY, JULY 11TH	
10:30 am – 11:15 am	Revolutionizing EDA: The Power of AI, ML, and NLP Majid Ahadi Dolatsara, Keysight Technologies
11:30 am – 12:00 pm	Achieving “System-Driven PPA” on Multi-Chiplet Designs Through Systemic Innovation Vinay Patwardhan, Cadence Design Systems
12:15 pm – 12:45 pm	Unleashing Semiconductor Innovation by Fostering Resilient Ecosystems Mahesh Deshpande, Dassault Systemes
1:00 pm – 1:45 pm	Are We There Yet? From Cloud-compatible to Cloud-optimized Natesan Venkateswaran, IBM; Richard Paw, Microsoft; Dean Hildebrand, Google; Murat Becer, Ansys; Amit Varde, Keysight
2:00 pm – 2:30 pm	Accelerate HPC/EDA Outcomes with an All-Inclusive and Efficient Data Life Cycle Management Plan Bikash Roy Choudry, Pure Storage, Inc.
2:45 pm – 3:15 pm	Solving the Problem for Hybrid Compute in a Hybrid Work Environment: Maximizing Employee Performance and Productivity while Reducing Costs and Protecting IP Rod Simon, OpenText
3:30 pm – 4:15 pm	Ask Me Anything with Ramki Balasubramaniam Ramki Balasubramaniam, AMD
4:30 pm – 5:00 pm	Intel PowerVia design considerations to optimize SOC design Craig Orr, Intel Foundry Services
5:15 pm – 5:45 pm	Have Your Cake and Eat It: Reliably Running Stateful Virtual Machines in Cheap Spot Markets. Hakim Weatherspoon, Exostellar, Inc.

TRANSFORMATIVE TECHNOLOGIES THEATER

Booth #1358

WEDNESDAY, JULY 12TH	
10:30 am – 11:15 am	Panel: Revolutionizing Chip Design: BAE Systems & Raytheon Collaboration Empowering Next-Generation Chip Design in the Cloud with Keysight Technologies and Microsoft Azure Dave Moser, BAE Systems; George Gerace, Raytheon Technologies; Joe Tostenrude, Microsoft; Amit Varde, Keysight Technologies
1:00 pm – 1:45 pm	Panel: Alternative Approaches to AI Chip Architectures Sally Ward-Foxton, EE Times; Prem Jonnalagadda, Lightelligence; Bo Beachler, Untether AI; Brucek Khailany, Nvidia
2:30 pm – 3:15 pm	Panel: Enabling AI at Zettascale: Wafers, Chiplets, or Both? Sally Ward-Foxton, EE Times; Ramin Fahjadrad, Eliyan; Ravi Mahajan, Intel; Charlie Wuischpard, Ayar Labs; Ian Cutress, More Than Moore

RISC-V ZONE THEATER SCHEDULE

Booth #2335



MONDAY, JULY 10TH

12:40 pm – 1:00 pm	Extending RISC-V with Custom Instructions Jon Taylor, Imperas Software Ltd.
1:40 pm – 2:00 pm	Why RISC-V is Inevitable Tiffany Sparks, RISC-V International
2:10 pm – 2:30 pm	Innovation by Collaboration: CHIPS Alliance Rob Mains, CHIPS Alliance
2:40 pm – 3:00 pm	Removing the Risk from RISC-V using the RISC-V Trace Standard Peter Shields, Tessent Embedded Analytics, Siemens
3:10 pm – 3:30 pm	A Digitally Wrapped Analog IP Subsystem for RISC-V Applications Chris Morrison, Agile Analog Ltd.

TUESDAY, JULY 11TH

12:10 pm – 12:30 pm	Caliptra: A CHIPS Alliance Work Group Prabhu Jayanna, CHIPS Alliance
12:40 pm – 1:00 pm	RISC-V Verification – Introduction to the Lost Art of Processor Verification Aimee Sutton, Imperas Software Ltd.
1:40 pm – 2:00 pm	Why RISC-V is Inevitable Tiffany Sparks, RISC-V International
2:10 pm – 2:30 pm	Creating Domain Specific Accelerators for RISC-V Designs with Siemens EDA Russell Klein, Siemens EDA
2:40 pm – 3:00 pm	A Digitally Wrapped Analog IP Subsystem for RISC-V Applications Chris Morrison, Agile Analog Ltd.
3:10 pm – 3:30 pm	Codasip's Data Driven Design Methodology Part 1 Keith Graham, Codasip s.r.o.
3:40 pm – 4:00 pm	Codasip's Data Driven Design Methodology Part 2 Keith Graham, Codasip s.r.o.

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