Japan

Chip design and EDA activities in industry, academia, and government

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I. INTRODUCTION

Japan stretches over a long distance from South to North, so the climate is quite different between its extremities. It is a very beautiful but small country. Its area is ranked 61st in the world. Japan is dependent on imports of agricultural products and natural resources.

Aging and energy issues are two major concerns. The proportion of elderly citizens is highest among advanced nations; more than 20% are over the age of 65 today. Huge damage was dealt to the Fukushima nuclear power plant from Tohoku earthquake and tsunami disaster on March 11, 2011. How to cope with our energy crisis is a serious problem.

Japan has world top class technologies such as the K super computer and the "Bullet Train" Shinkansen. K computer was first to achieve 10 PFLOPS performance in the world. Shinkansen has the safety record of no passenger fatal accident in 49 years with a maximum operating speed of 320 km/h.

The difference between Japanese and English languages is a great barrier for globalization. To overcome it, English became a compulsory part of the elementary school curriculum from April 2011 and many companies adopt TOEIC score for internal promotions.

II. INDUSTRY

Reorganization of the semiconductor industry is going in Japan. Toshiba, Renesas, Sony, Elpida, and Rohm are listed in the top 20 of 2012 semiconductor sales ranking. Their market share sums up to 20% though it was over 50% in the 1980s.

Japan has a long history of EDA R&D; many algorithms and methodologies were developed in both logic and physical design.

The Semiconductor Technology Academic Research Center, STARC[1], has played an important role in industry, government, and academia cooperation. STARC is a research consortium co-founded by major Japanese semiconductor companies in December 1995. It continuously strengthens semiconductor-related activities and research. Programs are "joint research with universities", "training of semiconductor design engineers", "development of basic design technology", and "support academia and industry by providing prototype

Capital	Tokyo
Largest city	Tokyo
Language	Japanese
Area Total	377,900Km^2
Population (Aug. 7, 2012)	126,659,683
Currency	Yen
Time zone	UTC+9
Internet TLD	.jp

fabrication services".

STARC achieved more than 500 joint researches with 41 universities in 15 years.

Japan Electronics and Information Technology Industries Association (JEITA) [2] is an industry group composed of over 400 companies. The EDA Technical Committee (EDA-TC) of JEITA is responsible for organizing and supporting events for the promotion of EDA technologies and standards. It will hold the Electronic Design and Solution Fair (EDSFair) from November 20 to 22, 2013 at Yokohama. It exhibits at DAC this year in booth #325 to promote new standard formats of LSI-Package-Board.

III.   ACADEMIA

The most important organization for VLSI design education in Japan is VLSI Design and Education Center (VDEC) [3]. It was established in University of Tokyo in May 1996.

VDEC aims at the advancement of researches and education on LSI design in universities. It sends many distinguished VLSI designers into the industry and holds seminars and forums to exchange opinions among young professors, students, and designers. After 15 years of VDEC, education on CAD software, LSI design and design flow in universities was greatly improved.

Now 153 universities and 640 research groups are members of VDEC and it has 9 branches in Japan. Over 1,000 papers are published through VDEC activities each year. Up to 404 chips were fabricated in 2004.

IV.   GOVERNMENT

The Japan Science and Technology Agency (JST) [4] under Ministry of Education, Culture, Sports, Science and Technology (MEXT) is one of the core institutions responsible for the implementation of science and technology policy in Japan. JST budget for FY2012 was ¥116.3B (~$1.13B). ¥55.8B (~$0.54B) was used for creating advanced technology and ¥28.9B (~$0.28B) was used for promoting technology transfer and innovation. Strategies of MEXT are based on "The 4th Science and Technology Basic Plan of Japan".

New Energy and Industrial Technology Development Organization (NEDO) [5] under Ministry of Economy, Trade and Industry (METI) is Japan's largest public R&D management organization. NEDO coordinates integration of the technological capabilities of private enterprises and development abilities of universities. It organizes mid- to long-term risk R&D as national projects. NEDO budget for FY2012 was ¥123.6B (~$1.2B). ¥109.2B (~$1.06B) was used for "National Projects" and the remaining for "Technology Seed Development Activities" and "Practical Application and Commercialization Promotion Activities".

REFERENCES
[1] http://www.starc.jp/index-e.html
[2] http://www.jeita.or.jp/english/
[3] http://www.vdec.u-tokyo.ac.jp/English/index.html
[4] http://www.jst.go.jp/tt/EN/about.html
[5] http://www.nedo.go.jp/english/index.html

Kaoru Kawamura graduated from Kyoto University and joined Fujitsu Laboratories Ltd. in 1979.
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