Power Gate Optimization Method for In-Rush Current and Power Up Time

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Post 90nm technology SOC low power dominated by sub-threshold leakage.

Decreasing the length of transistors from transistor scaling reduces the depletion channel length and hence increases the leakage current.

Sub-threshold leakage current also increases with temperature at each process node hence created a compounding effect.

Power Gating using MOS devices to form a switch between an external and internal power network is a well known and very effective technique to control leakages of logic gates.
Place and Route tool is used to pre-place the PFETs

- PFET is segmented into smaller PFETs distributed across whole power gated domain.
- PFETs are stitched and connected in serial to reduce in-rush current during power up.
Peak In-Rush current and voltage rail settling time is the key challenges on power gated design.

- In-Rush current consists of short circuit and leakage current. Long PFET chain increases voltage rail settling time.
- Data path connection from non-power up logics to power up logics increases short circuit current.
In-Rush Current Optimization Power Up Analysis Flow

- After Place and Route, the **PFET Stitching flow** is used to optimize the stitching direction.
- **PFET removal algorithm** is applied to improve the in-rush current.
- Power Up Analysis is done to collect the In-Rush current profile and voltage ramp up time.
- **IR-Drop Verification to verify no IR drop issue.**
1 way stitching method for PFET’s control. Only 1 chain is used.
PFET Stitching

- P (2) ways stitching method for PFET’s control.
- Total PFET chain Delay = N x T
  Where N = total number of PFET
  T = single PFET stage delay
- Number of PFET ways P = N x T / Treq
  Where Treq = Power Up Time Requirement
Prior publication by LK Yong and etc used Power Perimeter Scan (PPS) to scans for power gate load at its given perimeter / window and remove the PFETs located in the overlapping windows.

We use the driver-receiver pair list that had high short circuit power with PPS to determine if the PFET can be removed.

PFETs close to the receiver region will get higher cost function for removal.

PFETs close to the driver region will get lower cost function for removal.
## Results

<table>
<thead>
<tr>
<th>Description</th>
<th>Peak In-Rush Current (mA)</th>
<th>Power Up Time (ns)</th>
<th>Max IR Drop (mV)</th>
<th>Driver-Receiver Pair Violations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 way stitching</td>
<td>156</td>
<td>15.5</td>
<td>25</td>
<td>633</td>
</tr>
<tr>
<td>2 way stitching</td>
<td>279</td>
<td>7</td>
<td>25</td>
<td>255</td>
</tr>
<tr>
<td>1 way stitching with PFET removal</td>
<td>85</td>
<td>37</td>
<td>28</td>
<td>274</td>
</tr>
<tr>
<td>2 ways stitching with PFET removal</td>
<td>219</td>
<td>11</td>
<td>26</td>
<td>102</td>
</tr>
</tbody>
</table>

- 2 way stitching algorithm improves the power up time but increase the in-rush current.
- The PFETs removal algorithm is proven to be able to reduce the in-rush current.
- The max IR drop is kept within the 30mV budget specification range.
Summary

- The in-rush current during power up event is ascribed by both leakage and short-circuit current.

- Our proposal is able to reduce the in-rush current due to short-circuit current by clever avoidance on the voltage difference on drivers and receivers pair circuitry.

- The PFET stitching flow is also addressing the power up time concerns to reduce the power up time.

- Both the approaches are done without creating further IR Drop issue.

- The power up time and in rush current are affecting each other at the opposite way, the power grid designers will need to make the proper tradeoff to ensure the power gated design are meeting the product specified goal.