A Framework for Optimizing Thermoelectric Active Cooling Systems

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ABSTRACT
Thin-film thermoelectric cooling is a promising technology for mitigating heat dissipation in high performance chips. In this paper, we present an optimization framework for an active cooling system that is comprised of an array of thin-film thermoelectric coolers. We observe a set of constraints of the cooling system design. Firstly, integrating an excessive amount of coolers increases the chip package cost. Moreover, thermoelectric coolers are active devices, which dissipate heat in the chip package when they are in operation. Hence, setting the supply current level to operate the cooler improperly can actually lead to overheating of the chip package. Besides, the supply current needs to be delivered to the integrated cooler devices via dedicated pins. However, extra pins available on high-performance chip packages are limited. Observing these constraints, we propose an optimization framework for configuring the active cooling system, which minimizes the maximum silicon temperature. This includes determining the amount of coolers to deploy and their locations, the mapping of supply pins to the coolers, and determining the current levels of each pin. We propose algorithms to tackle the optimal configuration problem. We found that only a small portion of the silicon die needs to be covered by TEC devices (18% on average). Our experiments show that our algorithms are able to reduce the temperatures of the hot spots by as much as 10.6 °C (compared to the cases without integrated thermoelectric coolers). The average temperature reduction is 8.6 °C when 4 dedicated pins are available on the package. The total power consumption of the resulting active cooling system is reasonably small (~ 2 W). Our experiments also reveal that our framework maximizes the efficiency of the cooling devices. In the ideal case where hundreds of pins are available to tune the supply level of each individual cooler, the additional average reduction of the hot spot temperature is only 0.3 °C.

Categories and Subject Descriptors
B.7.2 [Integrated Circuits]: Design Aids

General Terms
Algorithms, Management, Performance, Design.

Keywords
Thermoelectric cooling, Thermal runaway, Optimization.

1. INTRODUCTION
Driven by the Moore’s law, the semiconductor industry has successfully doubled the integration density every two years for a few decades and is expected to continue its steady pace in the nanometer era. However, accompanied with the constantly elevated performance, the power density and operating temperature of high-performance chips keep increasing, posing challenges for the thermal design of the chip packages. Historically, the thermal design of the packages has been primarily guided by a single parameter, the thermal design power (TDP), which represents the maximum sustained power dissipated by the chips across a set of applications [1]. The past few decades have seen continual growth of the TDP. As the absolute TDP kept rising another phenomenon followed. The distribution of power densities of high-performance chips, particularly, microprocessor chips became highly uneven. At the hot spots, power densities can be as large as 300+ W/cm², while the average power density of the entire chip is normally an order of magnitude smaller [2, 3]. This phenomenon makes the TDP-based thermal design methodology, which accounts for the total power consumption only, insufficient to guarantee the safe operation of the microprocessors. Although scaling the TDP by a factor, which reflects the uneven power distribution, can address this issue, it may result in over cooling of large areas of the chip, leading to excessive package cost.

Active cooling technologies have shed new light on this matter. By incorporating miniature heat pumps [2-5], active cooling provides the capability of site-specific and on-demand cooling, promising new opportunities in cost-effective cooling. Among various active cooling techniques, thermoelectric cooler (TEC) has been the most accessible one. Discrete TEC elements have long been commercially available [6]. However, integrating such discrete TEC elements into the chip package for hot spot cooling is generally not an option, since the heat pumping capability of the discrete devices is limited due to the use of thin bulk thermoelectric materials [2]. Reducing the thickness of the thermoelectric materials help increase the heat pumping capability. For instance, it is shown that if the thickness of the TEC devices can be made to be less than 50 µm, it is possible to achieve the heat pumping capability of 500 W/cm² [2].

During the last couple years, significant advances in thin-film TEC have been reported in the literature. Venkatasubramanian et al. have demonstrated a 5 µm thick Bi₂Te₃ super-lattice TEC device which is estimated to achieve 500 W/cm² of cooling capability [5]. Böttner et al. have considered the monolithic integration of conventional bulk materials on silicon substrate [7]. They were able to deposit 20 µm legs using the integrated circuit fabrication process. A maximum cooling capability of ~ 100 W/cm² was reported. Snyder et al. proposed the embedded thermoelectric cooler (eTEC), which is about 100 µm thick and can be mounted on the heat spreader [4]. Recently, Chowdhury et al. have shown the integration of thermoelectric coolers fabricated from nanostructured Bi₂Te₃-based thin-film super-lattices into state-of-the-art electronic packages. An on-demand cooling swing of 7.3 °C is reported at the targeted region on a silicon chip with a local heat flux as high as 1300 W/cm² [2].

Although these progresses have paved the way for a new paradigm of cooling, many design trade-offs and constraints have to be considered. Firstly, the minimal region that needs to be covered by the TEC devices has to be determined, since integrating an excessive number of TEC devices increases the cost of the chip package. Secondly, the supply current levels of the TEC devices have to be set properly. Although the heat pumping capability of the TEC devices increases with their supply current, their power consumption increases at a faster pace. The power consumed by these devices would dissipate within the package, which could lead to overheating of the chip. Thirdly, dedicated current supply pins are needed in order to deliver the supply currents from the external sources to the integrated
TEC devices. The pin grid array on the modern high-performance microprocessors is quite crowded [8]. This situation would only become more severe in the future, since from generation to generation, the width of the data/address I/O buses increases, while the die size of each processor core keeps decreasing. Thus, the room for extra pins is scarce. Furthermore, within the package, the interconnects bridging the pins and the on-die I/O ports have been very dense [8]. Note that the typical supply current for a TEC device is in the order of a few Amperes. Thus, the interconnects carrying the supply currents have to be made wide enough to suppress the Joule heating effect. However, a wide interconnect would occupy a large routing area. Hence, multiple TEC devices need to be chained together and driven by one single pin so we can allocate as few extra pins as possible.

In this paper, we systematically study the optimization of the thin-film TEC based active cooling system considering the above-mentioned design constraints. In particular, given the number of available extra pins for the TEC devices, we investigate the optimal configuration of the active cooling system. This entails determining 1) the minimal deployment of the TEC devices, 2) the mapping of the dedicated current pins to the TEC devices, and 3) the proper supply current for each pin, such that the peak silicon layer temperature is minimized. We propose a three-phase optimization framework following the “relaxation and rounding” strategy to tackle this minimization problem. We have tested the optimization framework using various benchmarks. We observe that only a smaller fraction of the silicon area needs to be covered by the TEC devices (18% on average). We observe that our algorithms were able to bring down the temperatures of the hot spots by as much as 10.6 °C (compared to the cases without integrated TEC devices). Across a set of benchmarks, the average reduction of the hot spot temperature is 8.6 °C when 4 dedicated pins are available. Our experiments also reveal that the proposed algorithm can determine the system configuration under which the integrated TEC devices are utilized highly efficiently. Compared to an ideal case where hundreds of pins are available, the average reduction of the hot spot temperature in the 4-pin case is only 0.3 °C smaller. The total power consumption of the resulting cooling system is reasonably small (~ 2 W).

The remainder of the paper is organized as follows. Section 2 gives an overview of the related works. In Section 3, the principles of thin-film TEC based active cooling system are presented. We introduce the optimization framework for the cooling system in Section 4. Experimental results are presented in Section 5.

2. RELATED WORKS

There has been several early-stage works considering the optimization of individual TEC devices. Abramzon examines the optimal parameters (such as the height/area ratio) for a single TEC device using a numerical optimization approach [9]. Hou et al. propose an analytical framework to determine the optimal height of the TEC devices [10]. Wang et al. considered the optimization of embedded mini-contact enhanced TEC devices using a simulation based approach [11]. In particular, they examine the optimal current setting and mini-contact size of a TEC device embedded in a chip package using a finite element model. These works mainly concentrate on the optimization of the physical parameters of an individual TEC device. In contrast, our work focuses on the design and optimization of the entire cooling system considering the practical design constraints.

There are also researchers working on the thermal modeling of TEC devices. Sabounchi et al. considered the thermal model of TEC devices and proposed an equivalent thermal circuit diagram [12]. Mitrani et al. proposed both lumped and distributed SPICE models for TEC devices [13]. Both of these models involve complicated circuit elements such as voltage-controlled-voltage-source and temperature dependent heat source. In contrast, our proposed thermal model of the TEC device (Section 3.2) contains only thermal conductors and heat sources. This approach would simplify the steady state thermal analysis of the entire chip package.

In our previous work [14], we derived some fundamental theoretical results towards understanding the nature of the optimization problem for active cooling systems. We established a fundamental concept: the thermal runaway phenomenon. To be more specific, there exists a boundary for the supply current value beyond which the cooling system would exhibit thermal runaway. This preliminary study only concerned with a simple case where all cooling devices were supplied by a single current level. In this paper, we formulate a comprehensive framework tackling a practical and general cooling system optimization problem. Leveraging on the thermal runaway concept, we developed algorithms for our proposed three-phase optimization framework.

3. PRINCIPLES OF THIN-FILM THERMOELECTRIC COOLING SYSTEM

3.1 Basics of Thermoelectric Cooling

A thermoelectric cooler device consists of a couple of dissimilar semiconductor strips that are thermally connected in parallel (Figure 1(a)). According to the Peltier effect, when an electrical current $i$ is sent through them, heat is absorbed at one side and released at the other side. Denoting the heat flux and temperature at the cold (hot) side by $q_c$ ($q_h$) and $\theta_c$ ($\theta_h$), respectively, we have [13]:

$$q_c = \alpha \theta_c - \frac{1}{2} r i^2 - k (\theta_h - \theta_c)$$  \hspace{1cm} (1)

$$q_h = \alpha \theta_h + \frac{1}{2} r i^2 - k (\theta_h - \theta_c)$$  \hspace{1cm} (2)

where $\alpha$ is the Seebeck coefficient of the TEC device; $r$ and $k$ are the electrical resistance and thermal conductance of the device, respectively. The first term in these two equations describes the Peltier cooling effect. The second term is due to Joule heating that occurs in the TEC device – half of the Joule heat is dissipated at the cold side and the other half at the hot side. The third term is contributed by heat conductance from the hot side to the cold side. Subtracting $q_c$ from $q_h$ yields the input power of the TEC device:

$$P_{TEC} = q_h - q_c = r i^2 + \alpha i \Delta \theta$$  \hspace{1cm} (3)

The input power of the TEC devices would be dissipated within the chip package. Hence, an improper setting of the current levels would lead to the overheating of the chip package.

It is worth to note that although the above equations are widely used in the literature, they have omitted the Thompson effect, which accompanies with the Peltier effect [15]. The Thompson effect is
caused by the dependence of the Seebeck coefficient on temperature. However, the Thompson effect can be accounted for by substituting $\alpha$ with $(\alpha_H + \alpha_C)/2$, where $\alpha_H$ and $\alpha_C$ are the Seebeck coefficients at the highest and lowest allowable operating temperature of the system, respectively [15]. In our model, we have adopted this more accurate approximation.

Multiple TEC devices can be chained together to enhance the cooling effect (Figure 1(b)). Thin-film TEC devices normally occupy small areas. For instance, a thin-film TEC device proposed by Chowdhury et al. occupies 0.5 mm x 0.5 mm area [2]. The TEC devices are immersed in the thermal interface material (TIM) layer, lying between the silicon layer and the heat spreader (Figure 2).

### 3.2 Modeling the Chip Package with TEC devices

Based on the well-known duality between the heat transfer and electrical phenomena, the chip package can be modeled as a linear network consisted of thermal conductors [16] (thermal capacitors need to be included in the model also if the transient thermal behavior of the chip package is of interest). In order to construct the network, each layer of the package (the silicon layer, the TIM layer, the heat spreader and the heat sink) is dissected into smaller tiles. For each tile, a node is created in the linear network. Edges in the network represent the thermal conductance between the adjacent tiles. Power dissipations of the tiles in the silicon layer are modeled as current sources [16]. Validation of existing architecture-level thermal simulators has shown excellent agreement of the linear network model with the accurate finite element model [16, 17].

In order to incorporate the TEC devices into the linear network, we propose the following model for the TEC devices based on Equation (1) and (2) as depicted in Figure 3. A thermal conductor $\kappa$ connecting the two nodes models the term $\kappa(\theta_H - \theta_L)$ in Equation (1) and (2). The Joule heating effect (the second term) can be described by two heat sources connected to the hot side and cold side node, each having the magnitude of $\frac{V^2}{2}$. The Peltier heat $a(\alpha_H - \alpha_L)$, absorbed at the cold side can be described by a thermal conductor $a$ connecting the cold side and the hypothetical ground node which represents the absolute zero temperature. Likewise, the Peltier heat $a(\alpha_H - \alpha_L)$ released at the hot side can be modeled by a negative thermal conductor $-a$ connecting the hot side and the ground. Besides, we place two thermal conductors $g_H$ and $g_C$ at the hot/cold nodes to account for the contact thermal resistance between the device and the rest of the package.

Figure 4 illustrates the thermal model of the chip package with the TEC devices, where the notations SNK, SPD, and SIL represents the heat sink, the heat spreader, and the silicon layer, respectively. We note that as mentioned earlier, the TEC devices reside in the TIM layer. Here we have simplified the actual three-dimensional network to a two-dimensional one for ease of illustration. We note that the thermal model of the entire chip package is a linear network, since the thermal model of the TEC device contains only conductors and heat sources. Thus, standard linear network analysis techniques can be applied to study the thermal behavior of the package.

### 3.3 Chip Package Thermal Steady State Analysis

Cooling of the microprocessor chips is required in different environments including the functional test, burn-in, and user environment [1]. While during functional test, transient thermal management is needed, for the burn-in and user environment, steady state thermal management and analysis are generally sufficient [1].

In this section, we extend the standard nodal analysis technique [18] to compute the steady state temperature of the chip package with a fixed deployment and supply current setting of the TEC devices. As mentioned in the introductory section, we assume that there are a limited number of dedicated pins delivering the supply current for the TEC devices. Each pin supplies a chain of TEC devices as shown in Figure 1(b). We use a vector $\mathbf{i}$ to hold the supply current of each pin. Further, we notice that the power profile of the network depends on the input currents $i$, since the nodes representing the hot/cold sides of the TEC devices dissipate Joule power. We thus use a vector $\mathbf{p}(i)$ to hold the power dissipation of each node. Finally, we use notations $SIL, HOT, and CLD$ to denote the set of nodes in the silicon layer, the hot side, and the cold side of the TEC devices, respectively. Then, the steady state temperature profile $\theta$ can be computed by solving the following set of linear equations

$$G - D(i)\theta = p(i)$$

where matrices $G$ and $D$ are defined in the following

$$G = \begin{pmatrix} \sum_{j \in CLD} -g_H & \cdots & \cdots & \sum_{j \in SIL} -g_C \\ \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots \\ \sum_{j \in HOT} -g_H & \cdots & \cdots & \sum_{j \in SIL} -g_C \end{pmatrix}$$

$$D(i) = \begin{pmatrix} \alpha_H & \cdots & \cdots & \cdots \\ \alpha_C & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots \end{pmatrix}$$

In matrix $G$, $g_H$ is the thermal conductance between node $k$ and node $l$ ($g_H = 0$ if node $k$ and node $l$ are not adjacent). Matrix $D$ is a diagonal matrix where $\alpha_H$ is non-zero only when node $k \in HOT \cup CLD$. When $k \in HOT$, $\alpha_H$ equals to the product of the Seebeck coefficient $\alpha$ and the supply current of the corresponding TEC device; when $k \in CLD$, $\alpha_C$ would be the negative of the product of the Seebeck coefficient and the supply current.

### 4. COOLING SYSTEM OPTIMIZATION

In this section, we present a systematic approach to determine the cooling system configuration minimizing the peak silicon temperature.

#### 4.1 Problem Definition

**Problem 1 (Optimal Cooling System Configuration).**

Given:

1) a $pqg$ array of tiles representing the silicon layer of the chip where each tile has the same area as a TEC device,
2) the worst case power consumption of each tile, and
3) the number of pins $n_{pin}$ to deliver the TEC supply current;

Determine:

1) the set of tiles that needs to be covered by the TEC devices,
2) the mapping of the pins to the TEC devices, i.e., the set of TEC devices supplied by each pin, and
3) the supply current level of each pin;

**Objective**: The maximum steady state temperature of the silicon die is minimized for the given worst case power profile.

#### 4.2 Optimization Framework

We follow the “relaxation and rounding” strategy to solve the above problem. The optimization framework consists of three phases:
Phase 1. Problem Relaxation. We start by solving a “relaxation” of Problem 1, where in the relaxed case, 1) each tile is covered by a TEC device, and 2) the number of available pins is equal to the number of tiles. The rationale behind the relaxation is that if the conductivity of the TEC devices is larger than that of the TIM (which is the case in practice [2]), a TEC device with zero supply current would become a thermal conductor which conducts heat better than the TIM. As a result, the optimal solution of the relaxed problem places a lower bound on the achievable minimal peak silicon temperature. We have developed a search algorithm for the relaxed problem, which will be discussed in detail in Section 4.2.1.

Phase 2. Clustering based Current Pin Mapping. Our second and third phases “round” the solution of the relaxed problem to the solution of the original problem. As mentioned in the introductory section, the heat dissipation in the silicon layer is highly uneven. Only a small fraction of the tiles has high temperatures. Hence, in the solution of the relaxed problem, the supply current of most TEC devices would be zero. We first remove these TEC devices from the chip package. Then, the rest of the TEC devices are grouped into \( n_{pin} \) clusters. Here \( n_{pin} \) is the number of the pins dedicated for delivering the supply current from the external sources to the embedded TEC devices. This step determines the deployment of the TEC devices and the mapping between the pins and the TEC devices (Section 4.2.2).

Phase 3. Supply Current Level Setting. The last step of the “rounding” process is to determine the proper current level for each pin. The search algorithm in Phase 1 can be reused to determine the current levels (Section 4.2.3).

4.2.1 Search Algorithm for the Relaxed Problem

In the relaxed problem, each individual tile is covered by a TEC device and each individual TEC device is supplied by a dedicated current source. Thus, the thermal model of the entire chip package is constructed accordingly. Hence, we can formulate the relaxed problem as follows:

\[
\begin{align*}
\text{Minimize} & \quad \theta_{\text{max}} \\
\text{Subject to} & \quad \theta_k \leq \theta_{\text{max}}, \forall k \in \text{SIL} \\
& \quad (G - D(i))\theta = p(i)
\end{align*}
\]

(5)

(6)

The variable of the above optimization problem is the current vector \( \theta \), which holds the supply current of each pin. In Expression (6), the notation \( \theta_k \) refers to the \( k \)-th element of vector \( \theta \). It represents the temperature of node \( k \).

Let us first analyze the special properties of this problem. Our previous work has established the boundary for the supply current which causes thermal runaway in the single current pin case. This helps to refine the search space for the search of the optimal current value. In the following, we show that in the multiple pin case, the search space can be similarly restricted within a specific region.

**Theorem 1.** Define region \( R = \{ i \mid \text{matrix } G - D(i) \text{ is positive definite} \} \). Region \( R \) contains the zero vector \( (0, 0, \ldots, 0) \). As the current vector \( i \) approaches the boundary of \( R \), the steady state temperature of any node in the linear network approaches positive infinity. Here the steady state temperatures of the nodes are given by \((G - D(i))\theta = p(i)\) (Equation (4)).

**Sketch of Proof:** When \( i = (0, 0, \ldots, 0) \), each entry of \( D(i) \) is zero, and \((G - D(i)) = G\). It is known that \( G \) is a positive definite matrix [19]. Hence, the zero vector belongs to region \( R \).

Further, it can be shown that when matrix \( G - D(i) \) is positive definite, it belongs to a class of matrices which are invertible to matrices with all positive elements [20]. As \( i \) approaches the boundary of \( R \), matrix \( G - D(i) \) becomes closer and closer to a singular matrix. These two facts imply that all the elements in the inverse of \( G - D(i) \) approaches positive infinity as \( i \) approaches the boundary of \( R \).

The physical interpretation of this result is as follows. Each point at the boundary of the region \( R \) corresponds to a particular combination of input current levels which cause the active cooling system to have zero heat pumping capability. In the thermoelectric literature, this phenomenon has been known as the point at which coefficient of performance of the thermoelectric cooler becomes zero [21]. Since the cooling system stops pumping heat and the silicon layer still generates heat, thermal runaway of the system occurs.

The above discussion reveals that a current vector lying outside the region \( R \) is physically meaningless. Thus, we restrict the search of the current vector that minimizes the maximum silicon layer temperature within \( R \). We have developed a search algorithm to solve the problem defined by expression (5-6). The starting point of the search is the zero vector \( (0, 0, \ldots, 0) \). The search algorithm follows the gradient descent method [22] except that before taking each descending step \( \Delta i \) from the present point \( i \), we check whether vector \((i + \Delta i)\) is within region \( R \). If not, we reduce \( \Delta i \) by one half and repeat until \((i + \Delta i)\) is within \( R \). In order to check whether \((i + \Delta i)\) is within \( R \), according to Theorem 1, we only need to check whether \( G - D(i) \) is positive definite. This can be accomplished using the Cholesky decomposition algorithm \( O(n^3) \) time complexity) [22].

4.2.2 Clustering based Pin Mapping

In the first phase, we assume each tile is covered by a TEC device and determine the proper supply current for each individual TEC device. As we mentioned earlier, the uneven dissipation of heat in the silicon layer renders the supply currents of most of the TEC devices being zero. We can eliminate these TEC devices from the chip package. The supply currents of the remaining devices, when being plotted to a histogram, exhibit an interesting pattern. Figure 5 is an example of such a histogram based on the data extracted from our experiments. It shows the number of TEC devices in each “supply current bin”. It can be seen that there are four “naturally formed” clusters in the histogram. To explain these clusters, we note that to the first order of approximation, the supply current of a TEC device is determined by the temperature of its underlying silicon tile. The temperature of a tile in the silicon layer, in turn, is approximately determined by the power consumption of itself and its surrounding tiles. Furthermore, we note that tiles within the same functional unit usually have similar power consumption. This, plus the spatial correlation among them, indicates that the supply current levels of the TEC devices covering the same functional unit would be close to each other. They form a cluster in the supply current histogram. We apply the K-Means clustering technique [23] to group supply currents into \( n_{pin} \) clusters. The TEC devices in one cluster would be chained together and supplied by one dedicated current pin.

4.2.3 Supply Current Level Setting

Now, the actual deployment of the TEC devices and the current pin mapping has been determined in the second phase. Therefore, the thermal model of the entire chip package is now available. Thus, the problem of determining the optimal current levels, which minimize the maximum silicon layer steady state temperature, can be formulated exactly the same as Expression (5-6). Hence, we can reuse
the gradient descent based algorithm developed for the first phase to determine the appropriate supply currents of each pin.

5. EXPERIMENTAL RESULTS

5.1 Experimental Setup

We have implemented our optimization framework in C++ and evaluated the effectiveness and efficiency of the proposed algorithms on various benchmarks. All the experiments were carried out on a Linux server with a 2.8 GHz Intel® Core™ 2 Duo processors and 4 GB memory. In our implementation, the physical parameters (Seebeck coefficient, electrical resistivity) of the thin-film TEC device provided by Chowdhury et al. [2] are used. Other thermal modeling parameters such as the silicon thermal conductivity, convection, etc., were set according to an existing thermal simulator, HotSpot 4.1 [17]. We have first validated our thermal model without the TEC devices against HotSpot 4.1. For a given floorplan and a set of power traces, we performed steady state analysis using both our model and HotSpot 4.1 and compared the temperature of each tile generated by them. The two results agreed closely — the worst case difference is less than 1.5 °C. Next, we conducted experiments with our model including the TEC devices to evaluate the impact of the active cooling system on the thermal behavior of the chip package.

We carried out our experiments for microprocessors used in different working environments. We have used the SPEC2000 benchmarks suite [24] to generate power traces for a 65nm DEC Alpha-21364-like microprocessor. There are 19 applications, and we have used them to evaluate the effectiveness of the proposed algorithms.

5.2 Results and Discussions

Table II summarizes our experimental results. For each SPEC2000 benchmark set, we have listed the maximum steady state temperature of the silicon layer when no TEC device is integrated (Column “θ_{max}”), the number of TEC devices determined by our algorithm (Column “N_{TEC}”), and the percentage of the silicon die the TEC devices covers (Column “A%”). We have also provided the experimental results for different number of pins (Columns “1 Pin” through “4 Pins”), including the maximum steady state temperature of the silicon layer (Column “θ_{max}”), the reduction of the maximum temperature (Column “Δθ”), and the total power consumption of the integrated TEC devices (Column “P_{TEC}”). Finally, as a reference, we provide the same information for the relaxed case. In the relaxed case, each tile is covered by one TEC device and the supply current level of each TEC device is set in the first phase of our algorithm. Hence, it requires 144 TEC devices and 144 dedicated pins.

We notice that the number of tiles that needs to be covered by the TEC devices is comparatively small. For most of the benchmark sets, out of the 144 tiles in the silicon layer, less than 40 of them need to be covered by TEC devices. On average, only 18% of the silicon area needs to be covered. Figure 6 gives the deployment of the TEC devices.
devices for BenchSet4. For this benchmark set, only the heavily used functional units such as the floating-point and integer units need to be covered. Figure 6 also depicts the pin mapping for the cases where 2, 3 and 4 dedicated pins are available. As we mentioned in our discussion of the second phase of the optimization framework, the TEC devices covering the same functional unit tend to belong to the same cluster. Figure 6(d) depicts the pin mapping where 4 pins are available. In this case, the two TEC devices covering FPAdd belong to a cluster driven by pin 4. The two TEC devices on FPMul form another cluster supplied by pin 3. Most of the TEC devices on the IntExec and IntReg form the third cluster driven by pin 2. The rest of TEC devices belong to the fourth cluster supplied by pin 1. BenchSet4 is a floating-point intensive benchmark set. The functional units FPAdd and FPMul have power densities of 579.8 W/cm² and 463.4 W/cm², respectively, which are much higher than the power densities of other functional units. Besides, the gap between these two numbers is significant. Hence, when there are four pins available, the TEC devices covering these two functional units form two clusters. When there are two pins available (Figure 6(b)), TEC devices over these two units form one cluster and the rest form the other.

We observe that the reduction of the maximum temperature generally increases with the number of dedicated pins. On average, when there is only one pin available, an average reduction of 4.9 °C is observed. The average reduction increases to 7.8 °C, 8.3 °C and 8.6 °C when the available number of pins increases to 2, 3, and 4, respectively. For individual benchmark sets, the reduction can be as large as 10.6 °C when 4 pins are available (BenchSet4). For a few cases, the increase in the pin number actually yields less temperature reduction. For instance, for BenchSet4, when there are two pins available, the temperature reduction is 10 °C. However, when there are three dedicated pins, the reduction reduces to 9.6 °C. This is due to the heuristic nature of the “rounding” process in our algorithm.

We also observe the “diminishing return” effect. For instance, when the number of pins increases from 1 to 2, the increase in temperature reduction is 2.9 °C. However, increasing the number of pins from 2 to 3 only yields 0.5 °C temperature reduction on average. When there are 4 pins available, for each individual benchmark set, the temperature reduction is within 0.5 °C compared to that of the relaxed case. In the relaxed case where hundreds of pins are available to tune the supply level of each individual cooler, the additional average reduction of the hot spot temperature is only 0.3 °C. This indicates that our proposed optimization methodology is able to configure the cooling system in a highly cost-effective way.

We also evaluated the impact of the current level on the effectiveness of cooling. Figure 7 plots the peak temperature of the silicon layer as a function of the TEC supply current for BenchSet4. Here we assume only one pin is available and the deployment of the TEC devices is determined by our proposed algorithm. We observe that as the supply current increases, the peak temperature first decreases; however, beyond the optimal point, the peak temperature increases with the supply current. This result confirms that improper configuration of the supply levels may indeed cause the chip package to overheat.

Finally, in most of the cases, the power consumption of the integrated TEC devices is around 2 W. This is reasonable since the on-chip thermoelectric cooling technology is intended for high performance processors which can consume up to 100 W of power. We also note that the runtime of our algorithm is small enough. For any benchmark set and given number of dedicated pins, the execution time of our algorithm is less than 15 minutes. This amount of running time is acceptable since the proposed optimization algorithm only needs to be executed once in the chip package design flow.

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