DAC 2012 Keynote:
Designing a 22nm Intel® Architecture
Multi-CPU and GPU

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3rd generation Intel® Core™ processor (aka Ivy Bridge)

- First 22nm, 3-D Tri-Gate microprocessor
- Improved Performance & Responsiveness
- Power Efficient
- Better Graphics & Faster Media Processing
- Connected
3rd Generation Intel® Core™ Processor: 22nm Process

New architecture with shared cache delivering more performance and energy efficiency

** Cache is shared across all 4 cores and processor graphics
Ivy Bridge - Let's take a look inside...

- Continue the 2-chip platform partition (CPU + PCH)
- Fully integrated on silicon:
  - IA Cores, Processor Graphics
  - Media, Display engine
  - Memory Controller, PCI Express* controller
  - Modular on-die Ring Interconnect
  - Shared LLC
- Supports similar product offerings
- Backwards compatible socket (with 2nd Generation Intel® Core processor codename Sandy Bridge)
Ivy Bridge – Challenges

• Entire chip moves to 22nm
  - Higher performance/Lower power

• Graphics/Media
  - Higher 3D performance with next generation microarchitecture and Microsoft* DirectX*11
  - Up to 2X the graphics performance

• PCI Express 3.0
  - Double the speed: 12GB/sec I/O speed

• Security
  - Digital Random Number Generator
  - Supervisory Mode Execution Protection

• Power Management
  - Features for improved battery life

• Memory/Display
  - DDR3L support, improved overclocking
  - 3 independent displays
May 4, 2011

Intel announces intent to put a radically new transistor design into high volume production
Sandy Bridge vs. Ivy Bridge

<table>
<thead>
<tr>
<th></th>
<th>SNB</th>
<th>IVB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size</td>
<td>212 mm²</td>
<td>160 mm²</td>
</tr>
<tr>
<td>Total Transistors</td>
<td>1.16 B</td>
<td>1.40 B</td>
</tr>
<tr>
<td>Core Transistors</td>
<td>79.4 M</td>
<td>80.4 M</td>
</tr>
<tr>
<td>GFX Transistors</td>
<td>217 M</td>
<td>416 M</td>
</tr>
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Composition of CPU’s is Changing

Methods for developing and optimizing process technology need to keep pace with the product content.
22nm benefits

- Tri-gate device first time in HVM!
- Benefits include
  - Lower operating voltages/power due to exceptional low voltage delay scaling
  - 3 devices with different speed/leakage tradeoffs

Source: M. Bohr, K. Mistry IDF 2011
Key Capabilities/Methodologies

• **Design Re-use:**
  - Cell-based process migrations
  - Modular Graphics Design

• **Pre-planned and developed derivatives**
  - 4 dies from one base design

• **Parametric process technology evaluations**
Design Reuse: Cell-based Design Migration

Migration Principals:

- Joint process/design development to reduce effort to migrate process from 32nm to 22nm
- Speed/Power driven
- Preserve design assembly
- Cell based

Design Migration approach balances area/power scaling to achieve lower effort to converge design
MODULAR GRAPHICS DESIGN

• Graphics blocks modularly built
• Lower performance graphics derived from high performance graphics design
• Execution units, half slice and the cache banks modularly laid out.
Ivy Bridge Dies - Made for quick chops

4+2 → 2+2, 4+1, 2+1

First number is # of cores, second number is Graphics
IVB DIES  \[4+2 \rightarrow 2+2\]

- **X-chop areas for 1.5MB L2 (Last Level Cache)**
- **Y-chop areas for 2 core die options**

**IP Blocks (Re-use):**
- IA CORE (template)
- SA (System Agent)
- Display, GT2, GT1
IVB DIES – 4+2 ➞ 4+1

IP Blocks (Re-use)
IA CORE (template)
SA (System Agent)
Display, GT2, GT1

X-chop areas for 1.5MB L2 (Last Level Cache)
Y-chop areas for 2 core die options

core0, core1, core2, core3

GT2, GT1

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IVB DIES – 4+2 ➔ 2+1

IP Blocks (Re-use)
IA CORE (template)
SA (System Agent)
Display, GT2, GT1
IVB DIES - Made for quick chops

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IP Blocks (Re-use)
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X-chop areas for 1.5MB L2 (Last Level Cache)
Y-chop areas for 2 core die options
Process technology needs for CPU Core vs GFX

- **Core is architected to be a narrow & fast:**
  - Higher frequencies
  - Faster and bigger devices
  - Taller std-cell library
  - Dense power grid & Wider metals

- **Gfx is architected be wide & slow:**
  - Area & Leakage are more critical
  - Smaller and lower leakage devices
  - Shorter std-cell library
  - Dense layout & Narrower metals

- **Future Trend:**
  - Wider Engines (Frequency less critical)
  - Emphasis is on lower power through lower voltage
  - Shorter libraries, Denser layout & Narrower Metals
  - Higher variation especially for smaller devices
DFM Requirements & Tool Capabilities

- DFM rules are a key part of the equation for manufacturability:
- Many rules were guidelines but goal is to cover as much area as possible without increasing area.
- DFM represents a tradeoff between effort, die-area & manufacturability.

- Future trend:
  - DFM rules are getting more critical => No longer guidelines, but design rules & must fix!
  - Std-cell library & power grid design etc. need to comprehend them up-front.
  - Place & Route tools need to be “DFM aware”
Ivy Bridge Testing and Debug Capabilities

- Super high speed, parallel data loading for testing IA cores through DDR for functional/structural testing
- Ability to securely access every part of the chip through IEEE JTAG for control and debug
- Sophisticated PCIe debug hooks for logical state machine tracking and debug as well as analog circuit debug to cover for wide process window
- Extensive IO debug and testing capabilities including:
  - On die pattern generator, and Jitter margining to test high speed IOs like PCIe
  - Elaborate controls to tune IO ckt parameters
Ivy Bridge Emulation

- Pre-Si Emulation models available 3Q before TI
  - Many Pre-Si bugs found through emulation

- Emulation used in many areas:
  - BIOS boot checkout
  - RTL stress testing
  - GFX SV content checkout
  - GFX driver development
  - Test pattern validation
  - PCIe Gen3

- Benefits: Enabled Post Si Validation of Tock features in a Tick schedule

Emulation is trending to become a more significant piece of pre-silicon Hardware and software validation
22nm Test chip

Test chip helped enable process and design convergence

- Feedback to process and design teams
  - Passive elements, Transistor performance and leakage
  - Layout Design rules
  - Robustness and performance of process sensitive circuits

Test chip contents for process sensitive circuits

- PLLs: LC and self-biased types
- PCIe Gen3, DDR3 IOs
- Future Trends: To expand lead process test chip content to include densest standard cell libraries to understand yield impact

Final version of test-chip silicon 1.5 quarters before IvyBridge A-0 silicon

Lead process test chip with appropriate analog and digital content required for TTM
Summary

• Intel® Next Generation Microarchitecture, Codename Ivy Bridge, is another big leap in Performance/Power efficiency in both IA core and Graphics/Media

• Next generation Graphics microarchitecture is a Significant Graphics and Media (“tick+”) evolution for Intel® HD Graphics

• Designing a new process technology and product in parallel requires close interaction between design and technology teams

• Collaborative product and process technology development and optimization is key to achieving a winning product

It’s Just The Beginning
Additional Sources of Information on This Topic:

More web based info on Tri-Gate:

www.intel.com/technology/architecture-silicon/22nm/
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