DAC 2008 is seeking papers that deal with design tools, design methods, design techniques, and embedded design in a number of categories described below.

**Design Tools** papers describe contributions to the research and development of design tools and their supporting applications.

**Design Methods and Case Studies** papers describe innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art design projects.

**Design Techniques** papers describe the use of design tools and methods from the perspective of a specific design project. They include a brief description of the design and discussion of: methodology, flow, innovative use of tools, the limits of current tools, and what new tool capabilities are required for future designs.

**Embedded Systems** papers are characterized by mixed hardware and software components with limited resources. Increases in software content introduce new design issues. Embedded Design papers describe tools, methods, and case studies for applications with specific embedded system content.

**Wireless** is the theme topic for DAC 2008. Papers that specifically target wireless related design, verification, test and implementation issues will be highlighted at the conference.

### 1. System-Level Design and Co-Design
1.1 System specification, modeling, simulation, and performance analysis
1.2 Scheduling, HW/SW partitioning
1.3 Mapping, allocation
1.4 System-on-Chip (SoC) and Multiprocessor SoC (MIPSoc)
1.5 Application-specific processor design tools

### 2. System-Level Communication and Networks on Chip
2.1 Modeling and performance analysis
2.2 Communications-based design
2.3 Architectural synthesis, mapping, routing, scheduling
2.4 Optimization, power, energy, fault-tolerance, reliability
2.5 Interfacing and software issues
2.6 NoC Design methodologies and QoS flows, case studies

### 3. Embedded HW Design and Applications
3.1 Case studies of embedded system design
3.2 Flows and methods for specific applications and design domains
3.3 Low power design and thermal management
3.4 Embedded low-power approaches: partitioning, scheduling, and resource management
3.5 High-level power estimation and optimization
3.6 Gate-level power analysis and optimization
3.7 Device, circuit techniques for low-power design
3.8 Verification and testing
3.9 Functional, transaction-level, RTL, and gate-level modeling and verification hardware design
3.10 Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
3.11 Simulation and hardware simulators or accelerators engines
3.12 Modeling languages and related formalisms, verification plan development and implementation
3.13 Assortment-based verification, coverage analysis, constrained-random test bench generation
3.14 High-Level Synthesis
3.15 High-level, behavioral, algorithmic, and architectural synthesis, “C” to gate tools and methods
3.16 Mixed-SWI synthesis, communication network synthesis
3.17 Synthesis of digital circuits above the RTL level
3.18 Resource scheduling, allocation, and legalization
3.19 Logic synthesis and optimization (signal integrity, physical layout, simulation) beyond the die

### 5. System-Level Design and Co-Design
5.1 High-level, behavioral, algorithmic, and architectural synthesis, “C” to gate tools and methods
5.2 Physical design and thermal management
5.3 High-level power estimation and optimization
5.4 Gate-level power analysis and optimization
5.5 Device, circuit techniques for low-power design
5.6 Verification and testing
5.7 Functional, transaction-level, RTL, and gate-level modeling and verification hardware design
5.8 Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
5.9 Simulation and hardware simulators or accelerators engines
5.10 Modeling languages and related formalisms, verification plan development and implementation
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5.16 Resource scheduling, allocation, and legalization
5.17 Logic synthesis and optimization (signal integrity, physical layout, simulation) beyond the die

### 9. Logic Synthesis and Circuit Optimization
9.1 Combinational, sequential, and asynchronous logic synthesis
9.2 Library mapping, cell-based design and simulation
9.3 Translation and gate size and resource usage
9.4 Interactions between logic design and physical synthesis
9.5 Circuit simulation and Circuit Interconnect Analysis
10.0 Electrical circuit simulation
10.1 Model-order reduction methods for linear systems
10.2 Interconnect and substrate modeling and extraction
10.3 High-frequency and electromagnetic simulation of circuits
10.4 Thermal and electrothermal simulation
10.5 Timing Analysis and Design for Manufacturability
11.0 Design for yield, defect tolerance, cost issues, and imparts
11.1 Deterministic static timing analysis and verification
11.2 Performance analysis and optimization
11.3 Design for resilience under manufacturability simulations
12. Physical Design and Manufacturability
12.1 Physical Floorplanning, partitioning, placement
12.2 Buffer insertion, routing, interconnect planning
12.3 Physical verification and design rule checking
12.4 Automated synthesis of clock networks
12.5 Article enhancement, lithography related design optimizations
13. Signal Integrity and Design Reliability
13.1 Signal integrity, capacitive and inductive crosstalk
13.2 Reliability and modeling analysis
13.3 Novel clocking and power delivery schemes
13.4 Power grid robustness analysis and optimization
13.5 Soft-errors and single-event upsets (SEUs)
13.6 Thermal Reliability
14. Analog/Mixed-Signal and RF
14.1 Analog, mixed-signal, and RF design methodologies
14.2 Automated synthesis and macromodeling
14.3 Analog, mixed-signal and RF simulation and optimization
15. FPGA Design Tools and Applications
15.1 Rapid prototyping
15.2 Low power synthesis and physical design techniques for FPGAs
15.3 Configurable and reconfigurable computing
16. Testing
16.1 Test quality, reliability, correct-by-design, test delay, test power test
16.2 Digital fault modeling, automatic test generation, and prototyping
16.3 Digital design for test, test data compression, built-in self test
16.4 Test design for test and FPGA testing
16.5 Fault tolerance and on-line testing
16.6 Analog/mixed-signal RF testing, System-in-Package (SiP) testing
16.7 Board-level and system-level test, System-on-Chip (SoC) testing
16.8 Silicon debug, diagnosis, post-silicon design validation
17. New and Emerging Design Technologies, (including but not restricted to)
17.1 MEMS, sensors, actuators, imaging devices
17.2 Nano-technologies, nano-wires, nano tubes
17.3 Quantum computing
17.4 Biologically based or biologically inspired systems
17.5 New transistor structures and devices, new or radical processes
18. Special Theme Topic: Wireless
18.1 Emerging technologies for the design, verification, test and implementation of wireless systems
18.2 Power-aware and energy-efficient wireless protocols, algorithms and associated design techniques and methodologies
18.3 Embedded software design challenges for wireless applications and its impact on ESL design solutions
18.4 Promoting analog and mixed signal design techniques for wireless systems including but not limited to advanced antenna and RF design solutions

**New and Emerging Design Technologies**

**Special Theme Topic: Wireless**

**New and Emerging Design Technologies** - Emerging technologies for the design, verification, test and implementation of wireless systems

**Special Theme Topic: Wireless** - Embedded software design challenges for wireless applications and its impact on ESL design solutions

**Promoting analog and mixed signal design techniques for wireless systems including but not limited to advanced antenna and RF design solutions**
Dear Colleague,

I’d like to invite you to submit your work to next year’s Design Automation Conference (DAC) and get international recognition and prestige for work well done. The conference enables dialogue among peers and experts in our field. It is an opportunity for you to share your ideas and have a chance to win a Best Paper Award. Some new initiatives to encourage a broader audience include wireless and embedded design, Wild and Crazy Ideas – or WACI – Design Case Studies and a Design Contest. DAC is Where Electronic Design Meets! The Design Automation Conference is the world’s premier conference for the design of electronic circuits and systems. We look forward to hearing from you.

Limor Fix
General Chair, 45th DAC

**Eight types of submissions are invited:**

- Regular Papers
- Special Sessions
- Panels
- Tutorials
- Student Design Contest
- Workshops
- WACI
- Co-Located Events

Submissions must be made electronically at www.dac.com. Panel and tutorial suggestions, and special session submissions, are due no later than 5:00pm Mountain Time, November 1, 2007. Visit our website for complete information on the electronic submission process:

www.dac.com

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Special Session – Nov. 1, 2007
Panel & Tutorial – Nov. 1, 2007
Regular Papers – Nov. 19, 2007
WACI – Nov. 19, 2007
Student Design Contest – Dec. 5, 2007
Workshops – Feb. 15, 2008
Co-Located Events – Feb. 15, 2008

All submissions are due by 5pm Mountain Time