DAC 2016 Workshop on
System-to-Silicon Performance Modeling and Analysis
Power, Temperature and Reliability

Agenda

9:00 Welcome & Agenda
Adam Morawiec (ECSI, France)

9:15 Keynote 1: System Performance Modeling & Analysis in the Electronics Century
Eugenio Villar (University of Cantabria, Spain)

10:00 Session 1: System-Level Power and Temperature Specification, Modelling and Analysis
1.1 System-level Tracing, Monitoring and Analysis of Extra-Functional Properties
Achim Rettberg, (U Oldenburg & Hella AG, Germany)
1.2 Speed-Up in Design and Evaluation of Safety-Critical Systems based on UML-Profiles and IP-XACT (Case Study / Application Presentation)
Ralph Weissnegger (CISC Semiconductor, Austria)
1.3 Incremental Traceability Framework for Functional and Extra-Functional Properties in Embedded System Design
Emmanuel Vaumorin (Magillem Design Services, France)

11:00 Coffee Break

11:15 Keynote 2: Extra-Functional Properties Modelling Environment and Ecosystem
Laurent Maillet-Contoz (STMicroelectronics, France)

12:00 Keynote 3: Generic Multicore Enablement for Effective Programming
Andreas Herkersdorf (Chair for Integrated Systems, Technische Universität München, Germany)

12:45 Lunch

13:30 Keynote 4: Balancing the Effects of Process Variations, Aging, and Application Workload in Multi-Core Systems
Diana Marculescu (Carnegie Mellon University, USA)

14:15 Session 2: Ageing and Variation Effects Prediction
Organizers: *Christoph Sohrmann & Roland Jancke (Fraunhofer Institute for Integrated Circuits IIS, Germany)*
2. 1 Yield Analysis and Optimization of Full Custom Circuits considering Aging Effects
Michael Pronath (MunEDA, Germany)
2.2 Modeling Short and Long-term Effects of Aging from the Defect to Application Level
Victor M. van Santen, Hussam Amrouch and Jörg Henkel (Karlsruhe Institute of Technology, Germany)
2.3 NBTI Simulation for Aging of key Characteristics in Analog Circuits
Roland Jancke (Fraunhofer IIS/EAS, Germany)
2.4 Charge Trapping Phenomena in MOSFETS: From Noise to Bias Temperature Instability
Gilson I. Wirth (Universidade Federal do Rio Grande do Sul, Brazil)

15:35 Coffee Break

15:50 Session 3: Tool Support for Handling Ageing and Variation Prediction
3.1 Aging effects in Automotive Smart Power ICs
Roberto Stella (STMicroelectronics, Italy)
3.2 Modeling of Variability and Aging Effects Across Abstraction Layers
Adrian Evans (iROC Technologies, France)

16:30 End

DAC 2016 Workshop on
System-to-Silicon Performance Modeling and Analysis
Power, Temperature and Reliability

Rationale

The integration of heterogeneous electronic systems composed of SW and HW requires not only a proper handling of system functionality, but also an appropriate expression and analysis of various extra-functional properties: timing, energy consumption, thermal behavior, reliability, cost and others as well as performance aspects related to caching, non-determinism, probabilistic effects.

The workshop addresses cross-domain aspects related to the design and verification framework covering methodology, interoperable tools, flows, interfaces and standards that enable formalization, specification, annotation and refinement of functional and extra-functional properties of a system. Special emphasis will be given to formalization and expression of ***power, temperature, reliability, degradation and aging***.

Several research and industry efforts address (parts of) the problem. However, there is a need for community-wide cooperation to establish a holistic vision on extra-functional property treatment, and to agree on research and development directions and further on validation of applicable solutions and standardization.

This event will support collaboration between main actors from system and microelectronics industry, EDA and research.

The workshop is inviting submissions of short abstracts on industrial and scientific work in progress and practical solution and experiences.

Main topics

- Extra-functional property modeling (power, temperature, reliability, aging, …)
- Power and temperature analysis at SoC level: future needs and requirements
- Evolution and extensions of standards like UPF, IP-XACT to express extra-functional properties
- Power and temperature simulation and analysis at system-level
- System level reliability and aging models
- Reliability from transistor to RTL level: e.g. NBTI models including basic physical properties

Workshop Organizers:

- Laurent Maillet-Contoz, STMicroelectronics, France
- Kim Grüttner, OFFIS, Germany
- Gjalt de Jong, ArchWorks, Belgium
- Adam Morawiec, ECSI, France

Organized by R&D Collaborative projects:

Preliminary Agenda Structure

9:00 Welcome & Agenda

Adam Morawiec (ECSI, France)

9:15 Keynote 1: System Performance Modeling & Analysis in the Electronics Century

Eugenio Villar (University of Cantabria, Spain)

Abstract: Moore's Law has dominated the (re-)evolution of electronics during the last quarter of the XX century. All the electronic products we use today depend directly or indirectly on the increasing integration capability allowed by semiconductor technology. This evolution has enabled to produce new electronic products with unexpected capabilities just several years before they appear. The smart-phone and the tablet are examples of such products. This evolution still continues with wearables, bio-electronics, robots, drones, etc. Due to the pervasive character of electronics, electronic components are becoming fundamental in the improvement of many non-electronic products such as cars, airplanes, medical equipment, domestic appliances, etc. So, for example, in 2030, 50% of the value of a car is expected to be due to the electronics it contains. The influence of electronics goes further affecting most of the service sector. ICT services, ebanking, e-commerce, security, etc. have evolved dramatically as a consequence of the electronic push. A second consequence of Moore's Law affects the business model. All the electronic products, the electronic components in non-electronic manufactured products and services become obsolete in a short time as a new technology node is available able to produce devices with higher performance at the same cost.

Paradigmatic examples are the Intel's Tick-Tock and the iPhone evolution each year. The huge investments required to follow Moore's Law increases dramatically the cost of silicon and limits the accessibility to semiconductor fabrication to big players, both Integrated Device Manufacturers (IDM) and large Fabless semiconductor companies.

This business model will change in the short time as Moore's Law reaches an end. If Moore's Law changed gradually the world, its end may have a similar, but abrupt, effect. Cyber-Physical Systems of Systems (CPSoS) will dominate the electronics century becoming pervasive in all the aspects of our daily lives. For the first time, the underlying technology will be stable with only incremental improvements in time. This may make it accessible to many new players looking for a competitive advantage in silicon. Investment will move from the initial stages of the value chain to those closer to the final user. In this new scenario, modeling, analysis and verification of CPSs will have to evolve. The focus should be put on the device, not isolated but as a component in a complex, heterogeneous, distributed network of many other computing devices. Services will be offered by the interaction of functional components deployed in many distributed computing resources of many kind, from small motes, embedded systems and smart-phones to large data centers and even High-Performance Computing (HPC) facilities. Electronic design in this new context should address effectively new requirements. Among them, scalability, reusability, human interaction, easy modeling, fast design-space exploration and optimization, powerful functional and extra-functional verification, efficient handling of mixed-criticality and security, etc. An essential aspect will be the availability of powerful, platform independent SW and HW synthesis tools able to produce automatically efficient implementations of the system model on many different computing resources. In this presentation, the effect of this dramatic change in system design will be discussed. A single-source approach supported by powerful design tools will be proposed. Current results from the European FP7 ConTrex project will be described.

10:00 Session 1: System-Level Power and Temperature Specification, Modelling and Analysis

1.1 System-level Tracing, Monitoring and Analysis of Extra-Functional Properties

Achim Rettberg, (U Oldenburg & Hella AG, Germany)

1.2 Speed-Up in Design and Evaluation of Safety-Critical Systems based on UML-Profiles and IP-XACT (Case Study / Application Presentation)

Ralph Weissnegger (CISC Semiconductor, Austria)

Abstract: The electrification of today's vehicles and the high amount of new assistance features imply more and more complex systems. New challenges are arising through highly heterogeneous and distributed systems which interact with and have an impact on the physical world, so called cyber-physical systems. New Methods and tools are thus essential to support the development process and reduce costs and time-to-market, especially when systems are safety-critical and demand reliability. In this work, we present a novel method to

decrease design effort and speed up the evaluation process of safety-critical hardware. Due to the use of industry standards such as IP-XACT and UML/MARTE, high reusability of hardware and their associated failure-modes can be achieved, which makes old approaches in evaluation dispensable. Furthermore, our tool-aided methodology is tightly integrated into the design process. To demonstrate its efficiency, our methodology is applied to an industrial use case of a battery management system. The results show that using our approach, it is possible to decrease development time and effort in the development of safety-critical systems.

1.3 Incremental Traceability Framework for Functional and Extra-Functional Properties in Embedded System Design

Emmanuel Vaumorin (Magillem Design Services, France)

11:00 Coffee Break

11:15 Keynote 2: Extra-Functional Properties Modelling Environment and Ecosystem

Laurent Maillet-Contoz (STMicroelectronics, France)

12:00 Keynote 3: Generic Multicore Enablement for Effective Programming

Andreas Herkersdorf (Chair for Integrated Systems, Technische Universität München, Germany)

12:45 Lunch

13:30 Keynote 4: Balancing the Effects of Process Variations, Aging, and Application Workload in Multi-Core Systems

Diana Marculescu (Carnegie Mellon University, USA)

Abstract: How do natural systems endure and how is nature inherently resilient? Can we learn from the supreme engineer - nature - how to design systems that are either variation and aging-tolerant by themselves and in the presence of a diverse application workload? Electronic system design has benefited from decades of reliable and predictable functionality, but this trend is likely to slow down in future technology nodes. To support a path toward resilient computing systems, a holistic approach toward addressing energy awareness, reliability, and variability at all the levels in the system is required. This talk will discuss our work on achieving superior performance and power efficiency for silicon systems in the presence of challenges induced by manufacturing process or aging effects and will unravel applications of classic tool sets to the design and analysis of large scale real-life applications.

14:15 Session 2: Ageing and Variation Effects Prediction

Organizers: *Christoph Sohrmann & Roland Jancke (Fraunhofer Institute for Integrated Circuits IIS, Germany)*

Abstract: In almost all safety critical areas performance requirements are constantly increasing in order to provide the computing power for automating monitoring and control of the system's state and its environment. Applications areas include Automotive, Aviation, Medical, or Industrial, where the demand for highest performance at lowest energy consumption needs to be met together with an extended service life. These requirements can only be provided either by extremely scaled technology nodes or by further reducing the margins of today's technologies. In safety-critical applications, device failure cannot be tolerated. However, devices from advanced nodes or with low safety-margins are generally more susceptible to parametric deviations, either from process variations, parametric drift over lifetime or a combination thereof. The correct prediction of parametric deviations is therefore of uttermost important for future applications. This session features presentations on cutting-edge research on analysis methods for ageing and variation prediction in modern applications. The solutions presented will become the foundation of tomorrows IC verification tools. This session offers a platform to discussion and present tomorrow's reliability challenges.

2.1 Yield Analysis and Optimization of Full Custom Circuits considering Aging Effects

Michael Pronath (MunEDA, Germany)

Abstract: Aging effects such as HCI, NBTI, or TDDB, can be alleviated by tuning circuit device geometries with constraints on device degradation. There are many trade-offs between performance, area, power consumption, sensitivity to random process variation, and sensitivity to aging effects. We give an overview about such analysis and optimization methods for circuits designed in full custom design style such as I/O, analog/RF, and memories.

2.2 Modeling Short and Long-term Effects of Aging from the Defect to Application Level

Victor M. van Santen, Hussam Amrouch and Jörg Henkel (Karlsruhe Institute of Technology, Germany)

Abstract: Aging effects have become one of the major concerns when it comes to reliability. The physical causes behind them have been extensively studied in the last decade. However, research is still in its infancy with respect to modeling and investigating the ultimate impact of the generated defects at the application level, i.e. estimating the required guardbands for given applications to tolerate aging-induced degradations. This hold even more for the recently revealed short-term effects of aging.

In our work, we aim at investigating how efficient guardbands can be designed to sustain the reliability of on-chip systems. In our aging estimation, we take the well-known long-term effects of aging as well as the new short-term effects into account. Then, we abstract aging effects from the defect level all they to the application level. Furthermore, we propose new mitigation techniques addressing both long- and short-term aging in order to optimize guardbands.

For these purposes, we introduce a novel lightweight physics-based aging modeling, FPGA-based aging stimuli extraction platform and runtime gaurdband adaptation technique. Once aging-induced degradation is estimated, an aging-aware design flow can be obtained through building degradation-aware cell libraries. Our cell libraries can be used with existing commercial EDA tools to allow designers, for the first time, to automatically address aging concerns within their standard design flows..

2.3 NBTI Simulation for Aging of key Characteristics in Analog Circuits

Roland Jancke (Fraunhofer IIS/EAS, Germany)

Abstract: We apply a Negative Bias Temperature Instability (NBTI) model of switching-trap type to investigate the deterioration of key parameters in analog circuits subject to long-term NBTI stress. Our model is based on first-order kinetics of switching oxide traps and calibrated with measurements. It thus accounts equally for stress and recovery behavior even under multi-level stress pervasive in analog circuit operation. A novel extrapolation approach allows evaluating the threshold voltage shift at arbitrary future times without approximation but yet unprecedented efficiency. We have implemented the model into Cadence' Unified Reliability Interface (URI) facilitating aging simulation with RelXpert. Application of the model is demonstrated on the input offset voltage of a Miller op-amp and the frequency of a ring oscillator.

3.4 Charge Trapping Phenomena in MOSFETS: From Noise to Bias Temperature Instability

Gilson I. Wirth (Universidade Federal do Rio Grande do Sul, Brazil)

Abstract: MOSFET low-frequency noise is known to be dominated by charge capture and emission by defects (traps) close to the Si-SiO2 interface. It is also known to play a role in Bias Temperature Instability (BTI). A physics based modeling and simulation approach will be presented. It is based on the relevant microscopic quantities that play a role in both low-frequency noise (RTN) and BTI. The modeling approach is valid at both DC and large signal (AC) biasing, and may be applied to time domain (transient) and frequency domain (AC) analysis. At the beginning of the talk the basics mechanisms involved in charge trapping and de-trapping will be presented, including a critical discussion of key parameters such as trapping/de-trapping time constants and the amplitude of the fluctuations induced by single traps. Standard low-frequency noise models used today (e.g. BSIM) do not properly model noise behavior under large signal excitation, and often do not to properly model noise variability. The presented modeling approach is helpful in solving this issue. The role of charge trapping and de-trapping in BTI (Bias Temperature Instability) is also discussed and modeled. Mutual relation between the different reliability phenomena (low-frequency noise, BTI and random dopant fluctuations - RDF) is also studied. For instance, random dopant fluctuations (RDF) may exacerbate the impact of BTI and low-frequency noise on circuit performance. Moreover, low-frequency noise and BTI are emerging as potential yield hazards in the most advanced CMOS nodes, as it can for instance appear as a time dependent SNM limiter in SRAMs.

15:35 Coffee Break

15:50 Lessons Learned from Application of Handling Ageing and Variation Prediction

3.1 Aging effects in Automotive Smart Power ICs

Roberto Stella (STMicroelectronics, Italy)

Abstract: Smart Power Applications ICs aim at performing actuator functions in a very intelligent and controlled way after signal detection and processing. Smart Power ICs require dedicated technologies (such as BCD ones) able to integrate in the same chip analogic components (BJTs and LV MOS), digital components (CMOS), and power components (DMOS and HV MOS) needed for execution function. SP ICs are largely used for automotive applications such as engine control, fuel injection control, safety applications (Airbag, ABS, ESC etc.), lighting (LED drivers), electrical motors driving (mirrors, windows etc.), car radio power amplifier. The design of ICs for Smart Power Applications is very challenging due to the complexity of the involved electrical phenomena which must be accurately evaluated and effectively faced. In particular, Automotive applications requiring “zero excursion” devices need very robust design in order to yield circuits properly operating in all conditions without reliability issues.

A critical concern which must be very well managed is the aging of ICs elementary components when they are subjected to stressing electrical conditions. In order to design very stable circuits, it is mandatory to simulate accurately all degradation

mechanisms, such as Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI), in order to minimize the impact on circuit performances. This task can be accomplished using advanced features of circuit simulators (such as Eldo UDRM) even in the case of not standard advanced aging modeling.
The above topic will be discussed by showing examples coming from Automotive Smart Power Applications ICs with special emphasis on advanced modeling of HV MOS HCI and CMOS P-channel NBTI (including recovery effects).

4.2 Modeling of Variability and Aging Effects Across Abstraction Layers

Adrian Evans (iROC Technologies, France)

Abstract: There is a growing need to understand the impact of aging and variability early in the design cycle. This is especially true, in the quickly growing automotive market. In this talk, we review some of the key failure mechanisms that result from aging and variability, considering the relationship between time zero variability and aging related failures. We present some methodologies for tracking these effects at higher levels of abstraction including gate and RTL level. Finally, we share some proposals on advanced modeling techniques for analyzing the impact of faults at the system level.

16:30 End